COMPARATIVE ANALYSIS OF CAPACITOR CLAMPED MULTILEVEL INVERTER WITH AND WITHOUT FILTER USING THREE LEVEL SPACE VECTOR PULSE WIDTH MODULATION

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Abstract
Multilevel inverters are the preferred choice in industry for the application in high voltage and high power applications. Multilevel inverters has advantages over two level inverters like minimum harmonic distortion, reduced EMI/RFI generation, and operation on several voltage levels. This paper presents the analysis and comparison of a conventional three level Capacitor Clamped (CCM) multilevel inverter using three level Space Vector Pulse Width Modulation (SVPWM) and Sinusoidal Pulse Width Modulation (SPWM). For the two switching techniques simulations are carried out with and without filter. FFT analysis has been conducted to obtain the Total Harmonic Distortion (THD) for both SVPWM and SPWM outputs. The simulations are performed using MATLAB/SIMULINK software and the results are presented.
Keywords: Capacitor Clamped Multilevel Inverter CCI, Space Vector Pulse Width Modulation, Sinusoidal Pulse Width Modulation, Total Harmonic Distortion.

1. INTRODUCTION
When ac loads are fed through inverters it required that the output voltage of desired magnitude and frequency be achieved. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. If the dc input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse-width-modulation (PWM) control within the inverter [1].

The inverter which produce an output voltage of two levels are known as two level inverters. In high-power and high-voltage applications these two-level inverters however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and a machine drive for sinusoidal and trapezoidal current applications. This is where multilevel inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase power rating [2]. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized switching devices. The harmonic content of the output voltage waveform decreases significantly.

2. CAPACITOR CLAMPED MULTILEVEL INVERTER
The structure of this inverter is similar to that of the diode clamped inverter. Instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the capacitor clamped multilevel inverter is shown in Figure 1. This topology has a ladder structure of DC side capacitors. The voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the capacitor clamped multilevel based inverter is that it has
redundancies for inner voltage levels [2]-[5]. Unlike the diode clamped inverter, the capacitor clamped multilevel inverter does not require all of the switches that are ON (conducting) in a consecutive series. Moreover, the capacitor clamped multilevel inverter has phase redundancies, whereas the diode clamped inverter has only line-line redundancies. These redundancies allow a choice of charging and discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level $S_a=1$. Considering the direction of the a-phase capacitor clamped multilevel current $i_{ac1}$ for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. In Table 1, the current $i_{adc}$ is the a-phase component of the dc current [6]. The total dc current can be calculated by summing the components for all phases. As with the three-level capacitor clamped multilevel inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states that both capacitors can be regulated to their ideal voltages [7]-[9].

![Fig.1 Three level capacitor clamped multilevel inverter.](image)

<table>
<thead>
<tr>
<th>$S_a$</th>
<th>$T_a2$</th>
<th>$T_a1$</th>
<th>$V_{ag}$</th>
<th>$I_{ac1}$</th>
<th>$I_{adc1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>$V_{ac1}$</td>
<td>-1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$V_{dc} - V_{ac1}$</td>
<td>1</td>
<td>I$_{as}$</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>$V_{dc}$</td>
<td>0</td>
<td>I$_{as}$</td>
</tr>
</tbody>
</table>

Table 1 Switching of one leg of FCI

3. THREE LEVEL SVPWM

Space vector pulse width modulation is quite different from the other PWM methods. With PWMs, the inverter can be thought of as three separate push-pull driver stages which create each phase waveform independently. SVM however treats the inverter as a single unit. Specifically the inverter can be driven to eight unique states. Modulation is accomplished by switching the state of inverter [8]-[10].

In $\alpha-\beta$ coordinate axis, the space vectors corresponding to the 27 working states are shown in Fig.3. Due to the redundancy states the 27 switching states are really corresponding to 19 different space vectors. And they separate Fig.2 into 6 sectors A, B, C, D, E, F with 4 equilateral triangles in each sector. Fig.3 shows that through the calculations of the amplitude and phase angle, where the referred vectors locate can be decided [11]-[13]. For their symmetry, here only gives an example of sector A to describe how the referred ones integrated by basic vectors. No matter where $V_{ref}$ is, it can be expressed by

$$V_{ref} = (T_1V_1+T_2V_2+T_3V_3)$$  \hspace{1cm} (1)

$$T_1+T_2+T_3=T_s$$  \hspace{1cm} (2)

where $V_1, V_2, V_3$ - vectors that define the triangle region in which $V_{ref}$ is located.

$T_1, T_2, T_3$ – corresponding vector durations.

$T_s$ - sampling time.

![Fig.2 The space vectors corresponding to the 27 working state](image)

![Fig.3 The integration of $V_{ref}$](image)

Of all the 19 basic space vectors, there is one phase connected with zero curves at least except
long vectors, and forms the closed circuit with the plus or minus. As a result, the capacitors charge and discharge frequently, which causes the ripple of the neutral voltage. To make sure that the three-level circuit working under the normal condition, it is necessary to control the neutral voltage ripples acceptable. So it needs to consider about the influences reacting on it. The redundant small vectors separately exert plus and minus offset on the neutral voltage. For this reason, their acting time can be adjusted to keep the balance of the neutral voltages [14]-[16].

4. SINUSOIDAL PWM
This is a very simple technique for harmonic reduction. In this technique pulse magnitude will be constant and only pulse width can be changed. In this pure sine wave is compared with carrier wave and producing gate pulses.

Sine wave has fundamental frequency and carrier wave can be taken more than fundamental frequency Fig 4 shows Sinusoidal Pulse Width Modulation. Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave [17].

In the modulation techniques, there are two important parameters: frequency ratio,\( P = \frac{\omega_c}{\omega_m} \) modulation index \( M_a = \frac{A_m}{A_c} \) where \( \omega_c \) - reference frequency \( \omega_m \) - carrier frequency \( A_m \) - reference signal amplitude \( A_c \) - carrier signal amplitude.

In this method of modulation, several pulses per half-cycle are used. Instead of maintaining the width of all pulses, the width of each pulse is varied proportional to the amplitude of a sine wave evaluated at the centre of the same pulse [18]. By comparing a sinusoidal reference signal with a triangular carrier wave, the gating signals are generated.

The frequency of reference signal determine the inverter output frequency and its peak amplitude, controls the modulation index, M, and then in turn the RMS output voltage the more common carrier technique, the conventional sinusoidal pulse width Modulation technique, which is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform (natural sampling). The Fig.4 below shows the sinusoidal pulse width modulation for three level inverter [19].

5. FILTER DESIGN
A filter is required to obtain an approximate sine wave for the load, since the output of multilevel inverter is not sinusoidal. The filter is designed as per the equation:

\[
f_c = \sqrt{f_r f_s}
\]

\( f_c \) - corner frequency \( f_r \) - reference frequency
\( f_s \) - switching frequency

\[
f_c = \frac{1}{2\pi \sqrt{f_r}}
\]

6. RESULTS AND DISCUSSIONS
Comparison of SVPWM and SPWM fed three level capacitor clamped multilevel inverter with and without filter has been done using MATLAB/SIMULINK. The input for inverter is taken as 500 V. The switching of inverter was done by using both SVPWM and SPWM and total harmonic distortion was taken for both output voltage. Table 2 shows the simulation parameters.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dc} )</td>
<td>500V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>10kHz</td>
</tr>
<tr>
<td>( R_{load} )</td>
<td>1Ω</td>
</tr>
<tr>
<td>( L_{load} )</td>
<td>1mH</td>
</tr>
<tr>
<td>( C_{filter} )</td>
<td>10 ( \mu )F</td>
</tr>
<tr>
<td>( L_{filter} )</td>
<td>5mH</td>
</tr>
</tbody>
</table>

Table 2 Simulation parameters
The Fig.5 shows the Simulation of CCM. Fig.6 shows the output phase voltage of SPWM fed CCM inverter without filter and Fig.7 shows the output phase voltage of SPWM fed CCM inverter with filter. Fig.8 shows the FFT analysis of SPWM fed CCM inverter and from this it is clear that a THD of 32.27% and Fig.9 shows the output phase voltage of SVPWM fed FCI inverter without filter and Fig.10 shows the output phase voltage of SVPWM fed CCM inverter with filter.Fig.11 shows the FFT analysis of SVPWM fed CCM inverter and it shows THD as 19.71%.
REFERENCES


[16] Kalle Ilves, Antonios Antonopoulos, Staffan Norrga, Hans-Peter Nee, “A New...

