THEORETICAL ANALYSIS, COMPUTER SIMULATION OF A ZERO VOLTAGE TRANSITION SYNCHRONOUS BUCK CONVERTER FOR PORTABLE APPLICATIONS

Mary Florida[1], Asha Alice[2], Maria Jim Stony[3]
[1,2]Department of Mathematics, St.Xavier's Catholic College of Engineering.
[3]EEE Department, DMI Engineering College, Aralvaimozhi

Abstract
In this paper, a zero-voltage transition PWM synchronous buck converter, which is designed to operate at low output voltage and high efficiency typically required for portable systems. To make the DC-DC converter efficient at lower voltage, synchronous converter is an obvious choice because of lower conduction loss in the diode. The high-side IGBT is dominated by the switching loses and it is eliminated by the soft switching technique. Additionally, the resonant auxiliary circuit designed is also devoid of the switching losses. The suggested procedure ensures an efficient converter. Theoretical analysis, computer simulations are presented to explain the proposed schemes.
Index Terms: DC-DC Converter, IGBT, Switching loss, Synchronous Buck, Soft switching, ZVT.

1. INTRODUCTION

The next generation of portable products, such as personal communicators and digital assistants, has demanded improvement in dc-dc converter topology in order to increase battery life time and enable smaller, cheaper systems. Since many portable devices operate in low-power reserve modes for a majority of the time they are on, increasing light load converter efficiency can significantly increase battery life time. A key element in this task, especially at low output voltages that future microprocessor and memory chips will need, is the synchronous rectifier. The synchronous rectifier buck converter is popular for low-voltage power conversion because of its high efficiency and reduced area consumption. [3], [9], [12], [21], and [25]. A synchronous rectifier is an electronic switch that improves power-converter efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. **IGBT** usually serve this purpose.

However, high input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency. So in this paper we have optimized the efficiency of the synchronous buck converter by eliminating switching losses using soft switching technique. The voltage-mode soft-switching method that has attracted most interest in recent years is the zero voltage transition [1], [2], [4]-[8], [10], [11], [13]-[20], [22]-[24], [26]-[27], [29]. This is because of its low additional conduction losses and because its operation is closest to the PWM converters.

The auxiliary circuit of the ZVT converters is activated just before the main switch is turned and cease after it is consummated. The components in this auxiliary circuit have low rating as compare to main circuit. Because this circuit active in a fraction of switching cycle. Previously proposed ZVT-PWM converters have at least one of the following key drawbacks.

1) The auxiliary switch turned off while the current is conducting. This causes EMI and switching losses to appear that offsets the benefits of using the auxiliary circuit. . In converters such as the ones proposed in [2], [10],

[14] and [15] the turn off is very hard.

2) The auxiliary circuit causes the main converter switch to operate with a higher current stress and with more circulating current. This results in the need for a higher current-rated device for the main switch, and an increase in conduction losses. The converters proposed in [3], [6], [8], [11], [12], and [16] the current stresses are very high on the main switch

3) The auxiliary circuit components have high voltage and/or current stresses. Such as converters proposed in [1], [5], [6] and [13], [16]. The converter proposed in [23] and [28] reduces the current stress on the main switch, but circuit is very complex. Reducing switching losses for low power circuit such as synchronous buck is not known to be present in the literatures [1]-[24] and [26]-[29]

The converter shown in Fig.1 is designed for a low voltage, high current circuit and found to be highly efficient. Hence, this paper presents a new class of ZVT synchronous buck converter. By using a resonant auxiliary network in parallel with the main switch, the proposed converters achieve zero-voltage switching for the main switch and synchronous switch and zero-current switching for the auxiliary switch without increasing their voltage and current stresses.

This paper organized as follows: The next section gives review of the various modes of operation with their key waveforms and the representation of their equivalent operation modes. Section III presents the design considerations and Section IV includes simulation results of both open loop and closed loop. Section V includes some conclusions.

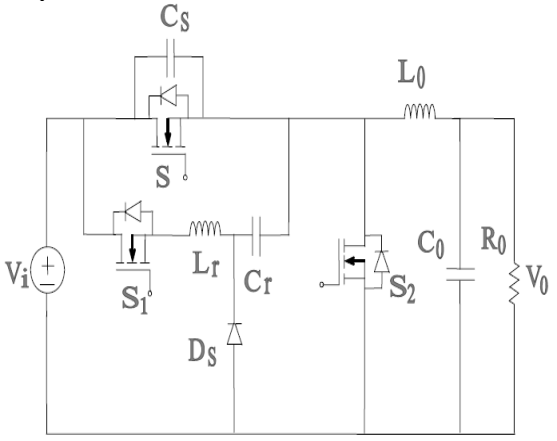

Fig. 1.1 Proposed converter circuit

2. ANALYSIS AND OPERATION PRINCIPLE

2.1. DEFINITIONS AND ASSUMPTIONS

The circuit scheme of the proposed new ZVT synchronous buck converter is shown in Fig.1.1 The auxiliary circuit consists of switch S1, resonant capacitor Cr, Resonant inductor Lr. The auxiliary circuit operates only during a short switching transition time to create ZVS condition for the main switch. The body diode of the main switch is also utilized in the converter. A high frequency schottky diode Ds is used for discharging the capacitor voltage to the output, which happens before the turn on of the synchronous switch. During one switching cycle, the following assumptions are made in order to simplify the steady-state analysis of the circuit shown in Fig.1.1.

- Input Voltage Vi is constant.
- Output Voltage Vo is constant or output Capacitor Co is large enough.
- Output Current Io is constant or output Inductor Lo is large enough.
- Output Inductor Lo is much larger than resonant circuit inductor Lr.
- Resonant circuits are ideal.
- Semiconductor devices are ideal.
- Reserve recovery time of all diodes is ignored.

2.2. MODES OF OPERATION

Eight stages take place in the steady-state operation during one switching cycle in the proposed converter. The key waveforms of these stages are given in figure 2.1. The detailed analysis of every stage is presented below:

Mode 1 (to, t1): Prior to t = t0, the body diode of S2 was conducting; main switch S and auxiliary switch S1 are turned-off. At t0, the auxiliary switch S1 is turned on which realizes zero-current turn-on as it is in series with the resonant inductor Lr. The current through resonant inductor Lr and resonant capacitor Cr rise at the same rate as falls of current through iS2.

Resonance occurs between Lr and Cr during this mode. The mode ends at t = t1, when iLr reaches I0 and iS2 falls to zero in result the body diode of S2 stops conducting. The voltage and current expressions which govern this circuit mode are given by:

$$iS2 = I0 - iLr \qquad (2.1)$$

$$iLr\,(t\text{-}t0) = \frac{Vi\ \mathrm{Sin}\,\omega\,(t\text{-}t0)}{Z} \qquad (2.2)$$

$\omega = \frac{1}{\sqrt{LrCr}}$ = Resonant frequency

$Z = \sqrt{Lr}/Cr$ = Characteristic impedance

$V_{Cr}\,(t1\text{-}\,t0) = V_{Cr1}$ (2.3)

$i_{Lr}\,(t_1\text{-}\,t_0) = I_0$ (2.4)

$$t_{01} = t_1 - t_0 = \frac{1}{\omega}\sin^{-1}\frac{(I_0 Z)}{(V_s)} \qquad (2.5)$$

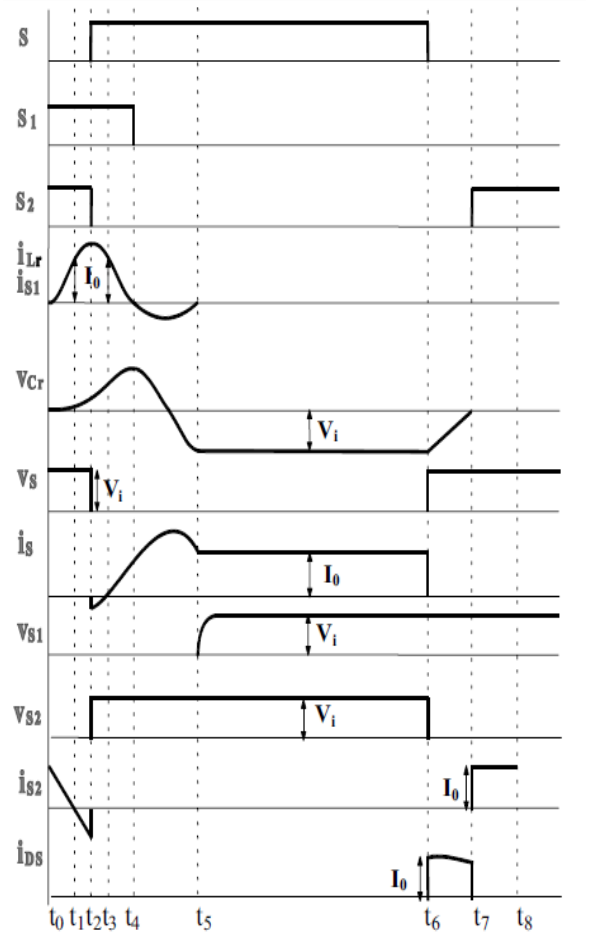

Fig. 2.1 Key theoretical waveforms concerning the operation stages.

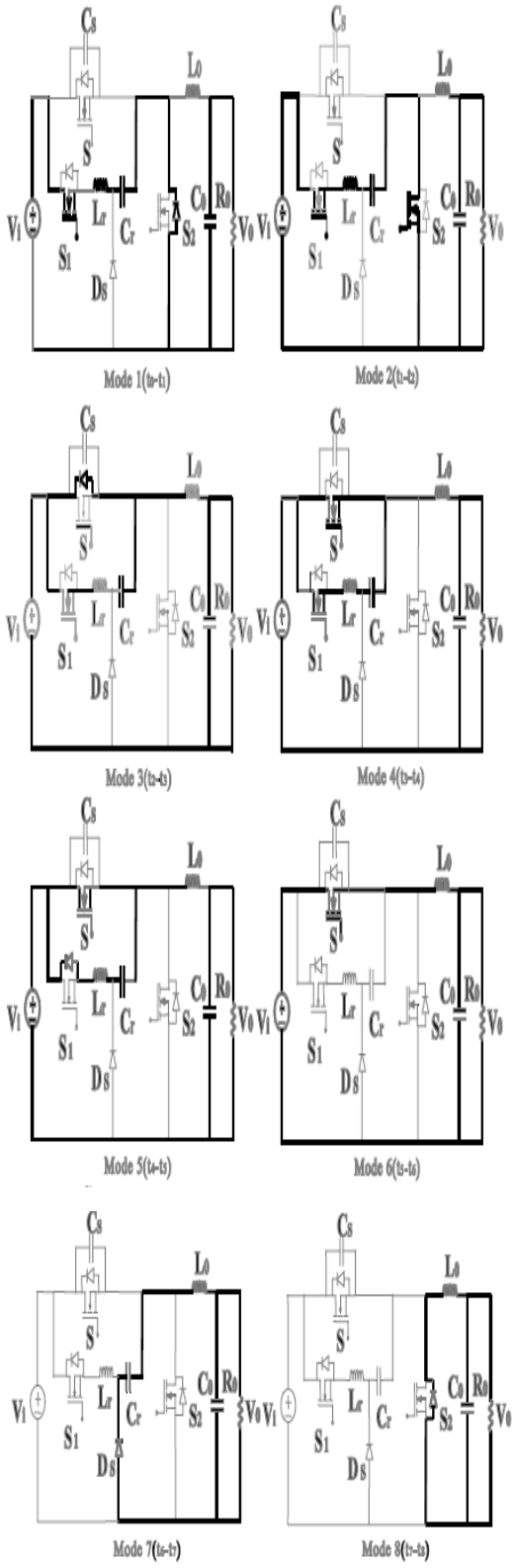

Fig 2.2 Modes of operations

Mode 2 (t1, t2): Lr and Cr continue to resonate. At t1, the synchronous switch S2 is turned on under ZVS. This mode is made to end by turning off the switch S2 under ZVS, when iLr current reaches to it maximum value i.e. iLrmax.

$$i_{S2} = i_{Lr} - I_0 \quad (2.6)$$

$$i_{Lr}(t-t_1) = \frac{V_s - V_{cr1}}{Z} \sin \omega (t-t_1) + I_0 \cos \omega (t-t_1) \quad (2.7)$$

At $t = t_2$,

$$i_{Lr}(t_2-t_1) = I_{Lrmax} \quad (2.8)$$

$$t_{12} = \frac{2}{\omega} \left\{ \tan^{-1} \frac{(V_s - V_{cr1})}{(I_0 Z)} \right\} \quad (2.9)$$

$$V_{cr}(t_2-t_1) = V_{cr2} \quad (2.10)$$

Mode 3 (t2, t3): At t2, iLr reaches its peak value iLrmax. Since iLr is more than load current I0, the capacitor CS will be charged and discharge through body diode of main switch S, which leads to conduction of body diode. This mode ends when resonant current iLr falls to load current I0. So current through body diode of main switch S becomes zero which results turned off of body diode. At the same time the main switch S is turned on under ZVS. The voltage and current expressions for this mode are:

$$i_{Lr}(t-t_2) = -V_{cr2}/Z \; Sin\, \omega (t-t_2) + I_{Lrmax} Cos\, \omega (t-t_2) \quad (2.11)$$

$$t_{23} = \frac{1}{\omega} \left[\tan^{-1} \frac{(I_{Lrmax} Z)}{(V_{cr2})} - Sin^{-1}(I_0) \right] \quad (2.12)$$

At $t = t_3$

$$i_{Lr}(t_{23}) = I_0 \quad (2.13)$$

$$V_{cr}(t_{23}) = V_{cr3} \quad (2.14)$$

Mode 4 (t3, t4): At t3, the main switch is turned-on with ZVS. During this stage the growth rate of is, is determined by the resonance between Lr and Cr. The resonant process continues in this mode and the current iLr continue to decrease. This mode ends when iLr falls to zero and S1 can be turned-off with ZCS. The voltage and current expressions for this mode are:

$$i_{Lr}(t-t_3) = \frac{-V_{cr3}}{Z} Sin\, \omega (t-t_3) + I_0 Cos\, \omega (t-t_3) \quad (2.15)$$

At $t = t_4$

$$i_{Lr} = 0 \quad (2.16)$$

$$t_{34} = \tan^{-1} (I_0 Z)/(V_{cr3}) \quad (2.17)$$

$$V_{cr}(t_4) = V_{cr\,max} \quad (2.18)$$

Mode 5 (t4, t5): At t4, the auxiliary switch S1 is turned off with ZCS. The body diode of S1 begins to conduct due to resonant capacitor Cr which starts to discharge. The resonant current iLr rises in the reverse direction, reaches a maximum negative and increases to zero. At this moment the body diode of S1 is turned off and the mode ends. The voltage and current equations for this mode are given by:

$$i_{Lr}(t-t_4) = \frac{V_{crmax} \, Sin\, \omega (t-t_4)}{Z} \quad (2.19)$$

At $t = t_5$

$$i_{Lr}(t_5) = 0 \quad (2.20)$$

$$t_{45} = \frac{\pi}{\omega}$$

$$V_{cr}(t_5) = -V_{cr4} \quad (2.21)$$

Mode 6 (t5, t6): Since the body diode of S1 has turned off at t5, now only the main switch S carries the load current. There is no resonance in this mode and the circuit operation is identical to a conventional PWM buck converter. The voltage and current equations for this mode are given by:

$$i_S = I_0 \quad (2.22)$$

$$i_{Lr}(t_6) = 0 \quad (2.23)$$

$$V_{cr}(t_6) = -V_{cr4} \quad (2.24)$$

Mode 7 (t6, t7): At t6, the main switch S is turned off with ZVS. The schottky diode D starts conducting. The resonant energy stored in the capacitor Cr starts discharging to the load through the high frequency schottky diode Ds for a very short period of time, hence body – diode conduction losses and drop in output voltage is too low. This mode finishes when Cr is fully discharged. The equations that define this mode are given by:

$$V_{cr}(t-t_6) = -V_{cr4} + \frac{I_0 (t-t_6)}{Cr} \quad (2.25)$$

At $t = t_7$

$$V_{cr}(t_7) = 0 \quad (2.26)$$

$$t_{67} = C_r V_{cr4} / I_0 \quad (2.27)$$

Mode 8 (t7, t8): At t7, the body diode of switch S2 is on as soon as Cr is fully discharged and schottky diode is turned off under ZVS. Dead time loss is negligibly small compared to the conventional synchronous buck converter.

During this mode, the converter operates like a conventional PWM buck converter until the switch S1 is turned on in the next switching cycle. The equation that defines this mode is given by:

$$i_{s2} = I_0 \qquad (2.28)$$

3.DESIGN PROCEDURE

Thus it is more significant to focus on design procedures of the auxiliary circuit. The resonant inductor, resonant capacitor, and the delay time of the auxiliary switch are the most important components when designing the auxiliary circuit. The proposed auxiliary resonant circuit provides soft switching conditions for the main transistor.

3.1.. DELAY TIME (TD)

The on time of auxiliary switch (S1) must be shorter than one tenth of the switching period.

TD =Ts/10 (3.1)

3.2. CURRENT STRESS FACTOR (a)

The current stress factor of the auxiliary switch is defined as

a = ILrm/Iin(max) (3.2)

but the limit of current stress factor is in between 1 to 1.5.

3.3 RESONANT CAPACITOR (Cr)

The resonant capacitor can be expressed as

(Cr)= (a-1)^2*Iinm*Td/[V0(1+pi/2(a-1)) (3.3)

3.4. RESONANT INDUCTOR (Lr)

The resonant inductor is given by

(Lr)=V0*Td/[Iinm(1+pi/2(a-1))] (3.4)

4. SIMULATION MODEL AND RESULTS

The Zero Voltage Transition Synchronous Buck converter can be implemented with the help of MATrix LABoratory [MATLAB] Simulink Version 2010a. The components of the circuit are taken from the Simulink tool box. The major parameters and components are given in table 1

Table 4.1: Simulation components

Components	Simulation values
Main switch, S	Ideal
Auxiliary Switch, S1	Ideal
Synchronous switch, S2	Ideal
Schottky Diode, Ds	Ideal
Capacitance, Cs	0.05nF
Resonant Inductor, Lr	200nH
Resonant Capacitor, Cr	0.2µF
Output Capacitor, Co	100µF

4.1. OPEN LOOP

Pulse generator generates the pulse for the switching devices with delay or without delay based on our requirements. The output voltage and other measuring instrument voltages and pulse are converted into graphical user interface by Scope. The Simulink model of Zero Voltage Transition Synchronous Buck converter is given by

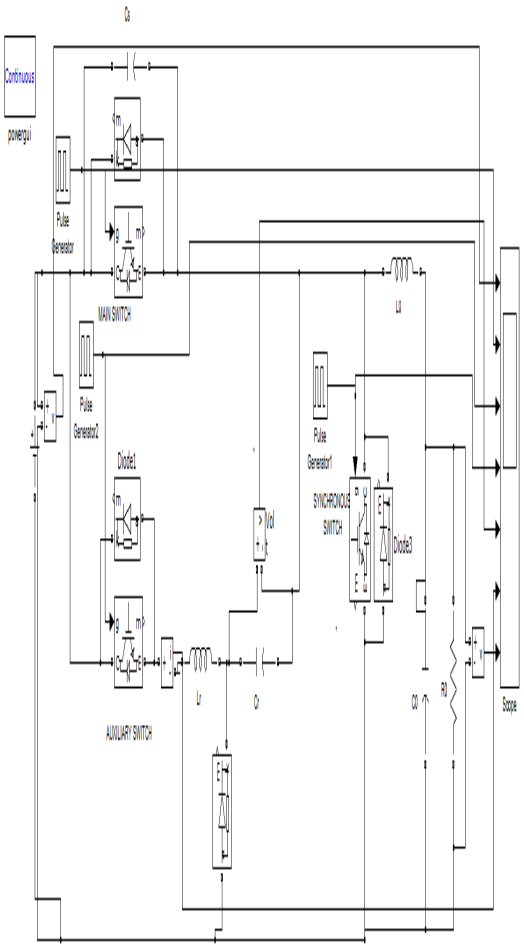

Fig 4.1 Open loop simulation

It consists of pulse generators, input voltage, resonant inductance and capacitance, output inductance and capacitance, resonant capacitor voltage ,resonant inductor current and output voltage.

When the inductor current reaches its maximum value, the voltage becomes zero, at this moment, the main switch get turn ON, its synchronous switch get turned OFF. The ZVS condition was achieved. When auxiliary switch is turned off when the inductor current reaches zero, hence ZCS condition was achieved too. When inductor current reaches its negative maximum, the voltage across Cr reaches its maximum value.

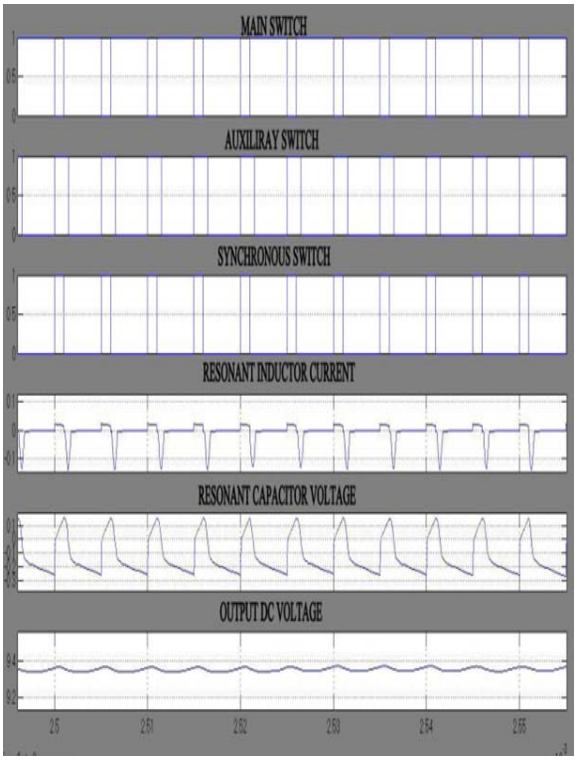

Fig. 4.2 Open loop waveform results

The fig 4.5 shows the status of switches, Resonant inductor current, capacitor voltage and output dc voltage of a Zero voltage transition synchronous buck converter with an input of 12 v of duty cycle 80% with a resistive load. The main and synchronous switches changed their status by zero voltage, termed as zero voltage switching. The auxiliary switch will turn off by zero current in the inductor. The switching frequency of all the IGBT are in 200Khz.The resonant frequency can be calculated from Lr, Cr values.

The output voltage is stepped down from the input voltage as the action of buck is achieved. The capacitor attains its maximum voltage, when the inductor crosses its negative maximum.

4.2. VARYING DUTY CYCLE

Load=100ohm, Input Voltage =12v

Table 4.2 Duty cycle Vs Output voltage

SL.NO	DUTY CYCLE(%)	OUTPUT VOLTAGE(V)
1	40	6.3
2	50	7.6
3	60	7.8
4	70	8.9
5	80	9.3

4.3. VARYING INPUT VOLTAGE

Load=100ohm, Duty Cycle=80%

Table 4.3 Input voltages

SL.NO	INPUT VOLATGE(V)	OUTPUT VOLTAGE(V)
1	10	7.7
2	12	9.3
3	15	11.7
4	20	15.8
5	24	19.0

4.5. CLOSED LOOP

The closed loop simulation result is given below

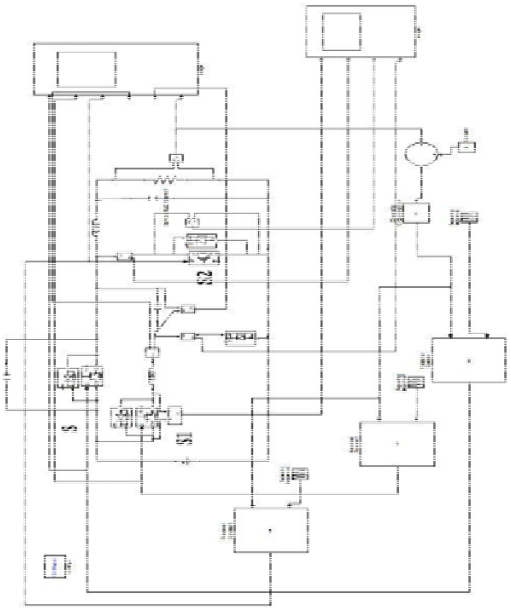

Fig 4.3 Closed loop simulation

In closed loop the output voltage will be compare to in one reference value. That reference value is given via relative operator.

4.6. VARYING VOLTAGE

The varying voltages with respect to the reference value in closed loop is given below table

Table 4.4 Varying Voltage

SL.NO	Vin (volt)	Vref (volt)	Vout (volt)
1	10	8	7.507
2	12	8	7.876
3	12	10	9.31
4	15	10	10.6

5. CONCLUSION

ZVS buck converter is an efficient step down DC-DC converter used in numerous electronics devices. Also the waveforms across capacitors and various test points were obtained, studied and compared with the theoretical waveforms. A ZVS Circuit was realized and its waveforms were observed. Parasitic capacitance of the transistor and the diode parasitic inductances of connections are all parts of the resonant circuit.

Switching of the transistor and the rectifying diode at zero voltage in the converter enables high operating frequency of the system while high energy efficiency is maintained. The range of the converter's operating frequency, in which ZVS switching is assured, is variable and dependent on the load resistance. ZVS buck converter generates dc voltage which can be applied in power supply system where high energy efficiency is required.

FUTURE SCOPE

To eliminate the errors, the output can be fed to the input through Fuzzy Logic controllers, so that the overall efficiency can be improved.

And also improve same via hardware implementation.

REFERENCES

[1]. L.Yang and C.Q.Lee, "Analysis and design of boost zero-voltagetransition PWM converter," in Proc. IEEE APEC Conf. 1993, pp.707-713.

[2]. G.Hua, C.S.Leu, Y.Jiang, and F.C.Lee, "Novel zero-voltagetransition PWM converters," IEEE Trans. Power Electron., vol.9, no.2, pp.213-219, Mar.1994.

[3]. A.J.Stratakos, S.R.sanders, and R.W.Broderson, "A low-voltage CMOSdc-dc converter for a portable battery-operated system," in Proc. Power Electronics Specialist conf., vol.1, Jun. 1994, pp.619- 626.

[4]. A.V.da Costa, C.H.G.Treviso, and L.C.deFreitas, "A new ZCSZVS-PWM boost converter with unity power factor operation," in Proc. IEEE APEC Conf., 1994, pp.404-410.

[5]. N.P.Filho, V.J.Farias, and L.C.deFreitas, "A novel family of DCDC PWM converters uses the self resonance principle," in Proc. IEEE PESC Conf., 1994, pp.1385-1391.

[6]. G. Moschopoulos, P.Jain, and G.Joos, "A novel zero-voltage switched PWM boost converter," in Proc. IEEE PESC Conf., 1995, pp.694-700.

[7]. Elasser and D. A. Torrey, "Soft switching active snubbers for dc/dc converters," IEEE Trans. Power Electron., vol. 11, no. 5, pp. 710–722, 1996.

[8]. K.M.Smith and K.M.Smedly, "A comparison of voltage-mode soft switching methods for PWM converters," IEEE Trans. PoElectron., vol.12, no.2, pp.376-386, Mar.1997.

[9]. O.Djekic, M.Brkovic, "Synchronous rectifiers vs. schottky diodes in a buck topology for low voltage applications," Power Electronics Specialists Conference, 1997. PESC '97 Record, 28th Annual IEEE, 22- 27 June 1997, vol.2, pp. 1374 – 1380.

[10]. Y.Xi, P.K.Jain, G.Joos, and H.Jin, "A zero voltage switching forward converter topology," in Proc. IEEE INTELEC conf., 1997, pp.116-123.

[11]. C.J.Tseng and C.L.Chen, "Novel ZVT-PWM converter with active snubbers," IEEE Trans. Power Electron., vol.13, no.5, pp.861-869, Sept.1998.

[12]. O.Djekic, M. Brkovic, A. Roy "High frequency synchronous buck converter for low voltage applications." IEEE PESC'98 Record, vol.2, pp. 1248 – 1254.

[13]. G. Moschopoulos, P.Jain, G.Joos, and Y.F.Liu, "Zero voltage switched PWM boost converter with an energy feedforward auxiliary circuit," IEEE Trans., Power Electron., vol.14, no.4, pp.653-662, Jul.1999.

[14]. T.W.Kim, H.S.Kim, and H.W.Ahn, "An improved ZVT PWM boost converter," in Proc. IEEE PESC Conf., 2000, pp.615-619.

[15]. J.H.Kim, D.Y.Lee, H.S.Choi, and B.H.Cho, "High performance boost PFP with an improved ZVT converter," in Proc., IEEE APEC Conf., 2001, pp. 337-342.

[16]. N.Jain, P.Jain, and G.Joos, "Analysis of a zero voltage transition boost converter using a soft switching auxiliary circuit with reduced conduction losses," in Proc. IEEE PESC Conf., 2001, pp.1799-1804.

[17]. M.L.Martins, H.A.Grundling, H.Pinheiro, J.R.Pinheiro, and H.L. Hey, " A ZVT PWM boost converter using auxiliary resonant source," in Proc. IEEE APEC Conf., 2002, pp.1101-1107.

[18]. C.M.Wang, "Zero-voltage-transition PWM dc-dc converters using a new zero-voltage switch cell," in Proc. IEEE INTELEC Conf., 2003, pp.784-789.

[19]. M.L. Martins, J.L. Russi, H. Pinheiro, H.A. Grundling, H.L. Hey, " Unified design for ZVT PWM converters with resonant auxiliary circuit," Electric power applications, IEE proceedings, vol.151, issue 3, 8 May 2004, pp. 303-312.

[20]. S. Kaewarsa, C. Prapanavarat, U. Yangyuen, "An improved zerovoltage-transition technique in a single-phase power factor correction circuit," International conference on power system technology – POERCON 2004, 21-24 Nov. 2004, vol.1, pp.678 – 683.

[21]. M.D.Mulligan, B.Broach, and Thomas H.Lee," A constantfrequency Method for Improving light-load efficiency in synchronous buck converters," IEEE Power Electronics letters, vol.3, no.1, pp.24-29, March 2005.

[22]. M.L.Martins, J.L.Russi, H.L.Hey, "Zero-voltage transition PWM converters: a classification methodology," IEEE proceedings on electric power applications, 4th March 2005, vol.152, no.2, pp.323 – 334.

[23]. W.Huang and G. Moschopoulos, "A new family of zero-voltage transition PWM converters with dual active auxiliary circuits," IEEE Trans. Power Electron., vol.21, no.2, pp.370-379, March 2006.

[24]. V.Yousefzadeh and D.Maksimovic, "Sensorless optimization of dead times in dc-dc converters with synchronous rectifiers," IEEE Trans. Power Electronics, vol.21, no.4, pp.994-1002, July 2006.

[25]. A.K. Panda, Aroul.K, "A Novel Technique to reduce the Switching losses in a synchronous buck converter" IEEE PEDES Conference, 12th-15th Dec2006, IIT, Delhi, pp.1-5.

[26]. B. P. Divakar; D. Sutanto, "Novel topologies for DC-DC converter with PWM control," International Journal of Electronics, Volume 87, Issue 6 June 2000 , pages 741 – 756.

[27]. Shui-Sheng Qiu; Igor M. Filanovsky; Bo-Tao Lin, "A new method of analysis for PWM switching power converters," International Journal of Electronics, Volume 86, Issue 11 November 1999 , pages 1395 – 1410.

[28]. Sam ben-yaakov; gregory ivensky; oleg levitin; alexander trainer, "Optimization of the auxiliary switch components in ZVS PWM converters" International Journal of Electronics, Volume 81, Issue 6 December 1996 , pages 699 – 712.

[29]. Gun-Woo Moon, "Design of high efficiency interleaved active clamp zero voltage switching forward converter" International Journal of Electronics