DESIGN OF CAPACITIVE DAC BASED SUCCESSIVE APPROXIMATION A/D CONVERTER

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Abstract

The purpose of this paper is to design a 12 bit SAR Analog to Digital converter using 180nm technology working with a supply voltage of 1.8v. The proposed ADC structure has applications in many fields for data acquisition. A N-bit SAR ADC can give 2^N digital output values which implies a minimum of N flip flops are needed. In this paper, a C-2C DAC based SAR is used when compared to the conventional resistive DAC as it consumes less power and mitigates the mismatch errors.

Keywords: ADC- Analog to Digital Converter, DAC-Digital to Analog Converter, DFF- Data Flip Flop, SAR- Successive Approximation Register.

I. INTRODUCTION

Transformation of continuous analog signal to digital signal is accomplished by an ADC. Digital signals are reliable and hence are used frequently. Digital systems dealing with digital signals are easy to design, has minimum effect on it due to variations in supply, accurate and have less effect of noise. Analog to Digital converters finds it's applications in acquiring of data, interfacing of sensors, RADAR, medical fields etc.

The Successive Approximation ADC follows the algorithm described below- Conversion is done based on the concept of binary search. Firstly, the successive approximation register is cleared. At the start of clock cycle the MSB is set to 1 and all the others bits are set to 0. If the output of DAC is greater than the applied input voltage then clear the MSB back to 0 else set the next MSB to 1. This process is continual until conversion is completed . When the last flip flop's output is high then this process comes to a halt and the digital data stored in the register corresponds to the digital equivalent of the given input analog signal. As shown in the block diagram Fig.1, SAR control logic, DAC, Comparator and Sample and Hold circuit blocks together constitute SAR ADC. The working of each block is explained below in detail with respective block diagrams and circuitry.

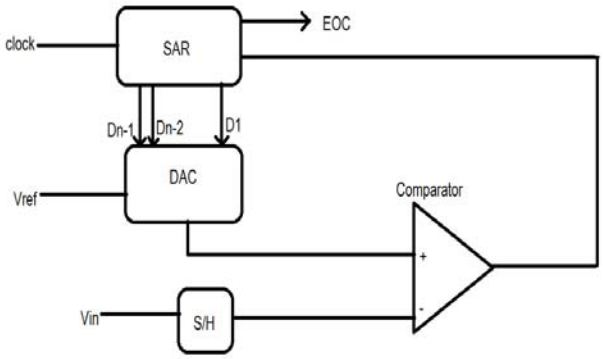

Fig.1: The standard SAR ADC architecture

II. CIRCUIT DESCRIPTION

A. Sample and Hold circuit:

This circuit samples the input and retains this value until the next sampling interval. Here in this circuit, a NMOS is being used as a switch which can be controlled by a signal Vpulse, and a capacitor which serves as a storage element.

As seen in Fig.2, the input Vin is applied to the drain of the NM1 MOSFET. The signal which controls the sampling action is applied to the gate. When the control signal is high, the transistor is on and provides a low resistance short circuit path, thereby charging the capacitor. Thus, applied input appears at output. This is the sampling phase. When the control signal becomes low, NM1 is in off state and breaks the circuit. The second phase is the hold phase during which the capacitor discharges. The frequency of the control signal is higher than that of the input signal to get a approximate version of input.[1]

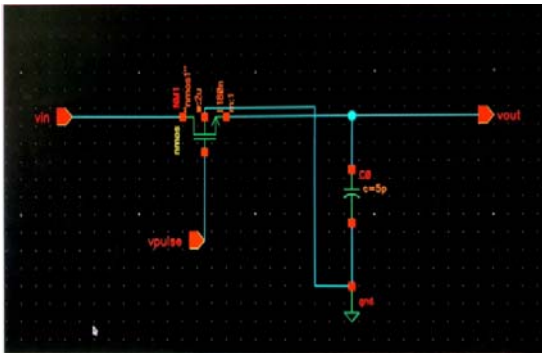

Fig.2: Sample and Hold circuit schematic

B. SAR control logic

The vital block in the architecture of SAR ADC is the control logic. The main building block of the control logic is the positive edge triggered D flip flop. These D flip flops along with OR gates perform successive approximation. A edge triggered D flip flop with active high asynchronous inputs inputs is built to implement SAR control logic. The registers in the lower part form a simple shift register whereas the upper flip flops form an array which stores the comparator output. When start of conversion (SOC) signal is high, the first flip flop of shift register is set and all the other flip flops are cleared to 0. The shift register is loaded with 10000 and array gives 0000. The OR logic gives the value 1000 at output (Q3-Q0). After the first clock pulse, the shift register now bears 01000 and the SAR output would be C000 where C is the comparator output. This process is reiterated till the output of SAR becomes $C_3C_2C_1C_0$. The output of extra flip flop in shift register is END (End of conversion) which, when high indicates that the digital output could be read in next pulse.

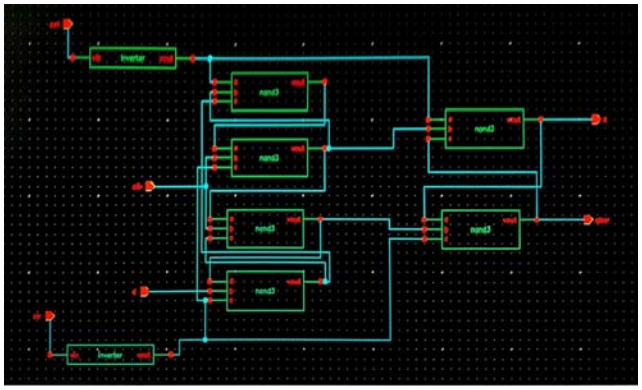

Fig.3: D flip flop schematic

The working of SAR control logic is explained using

Table 1 -

Table1: Working of SAR algorithm

Cycle	Q3	Q2	Q1	Q0	Comp
0	0	0	0	0	-
1(SOC high)	1	0	0	0	C3
2(clock)	C3	1	0	0	C2
3(clock)	C3	C2	1	0	C1
4(clock)	C3	C2	C1	1	C0
5(clock)	C3	C2	C1	C0	-

The schematic of the above described SAR control logic is given in Fig.4 [4].

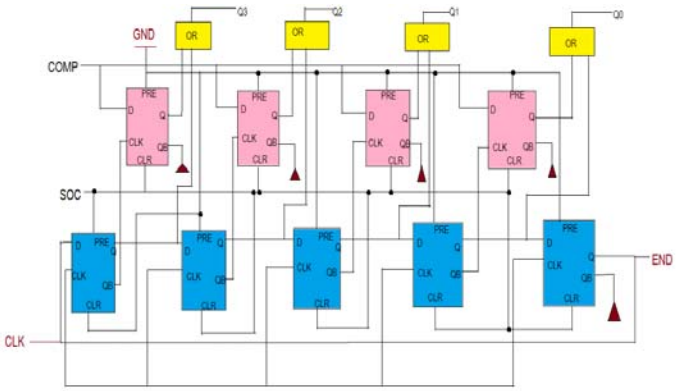

Fig.4: SAR Control Logic

All the above individual blocks are combined together using their symbols which have been created as shown in fig.5.

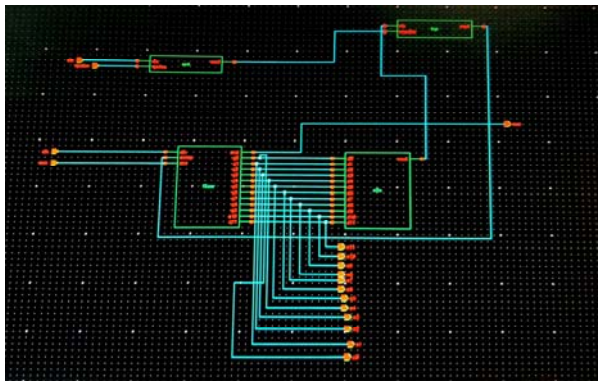

Fig.5: SAR ADC architecture

C. DAC circuit

A device which coverts digital signal to analog signal is termed as Digital to Analog Converter. DACs are used in ADCs to determine it's linearity. C-2C type capacitor based DAC is used in the design of ADC as the consumption of power is less in these type of DACs and mismatch errors are less in comparison to the resistor based R-2R DAC .Also, the conversion in C-2C DAC is faster.

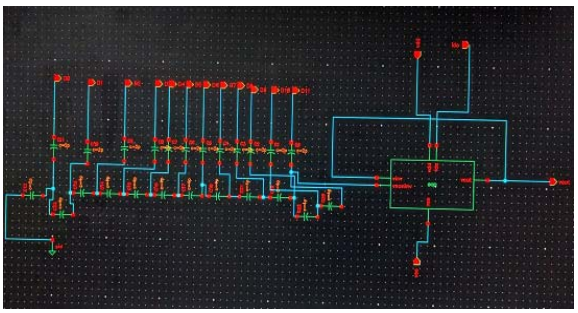

Fig 6: 12 bit DAC schematic

D. Comparator

Comparator compares the inputs of inverting and non-inverting terminals and based on the functionality it gives logic 1 or logic 0 as output. The output is logic '1' when the difference between the inputs is positive and the output is logic '0' when the difference is negative. A two stage operational amplifier consisting of 8 transistors is used in this design which serves as a comparator. The first stage includes a pair of nmos transistors which form input differential amplifier and a pair of pmos transistors which form active load. To bias the input differential stage, a current mirror is used with reference current Ibias =30uA. The nmos transistors NM3 and NM4 make up the current mirror. The second stage is the output stage formed by a common source amplifier which consists of transistor *NM2*. Bias current is provided for transistor NM2 by using another transistor PM2 which will acts as active load. To provide stability, 1pF capacitor is used at the output stage. [3]

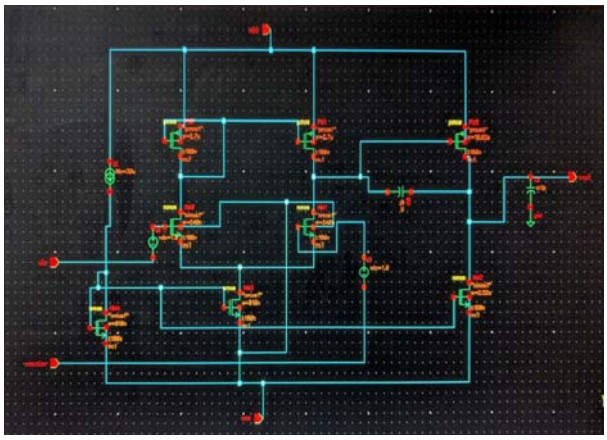

Fig. 7: Two stage op-amp schematic

III. SIMULATION AND RESULTS.

All the above circuits are simulated using cadence software and the outputs of comparator, SAR logic, Digital to Analog Converter and sample and hold are shown below. All these blocks are integrated together to form final architecture of Successive Approximation ADC and the output of this is also given below.

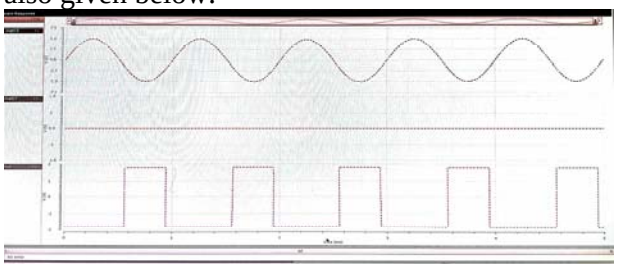

Fig.8: Comparator output

Fig.8 shows the output of comparator in which two inputs are compared and based on the operation described above, the outputs are obtained.

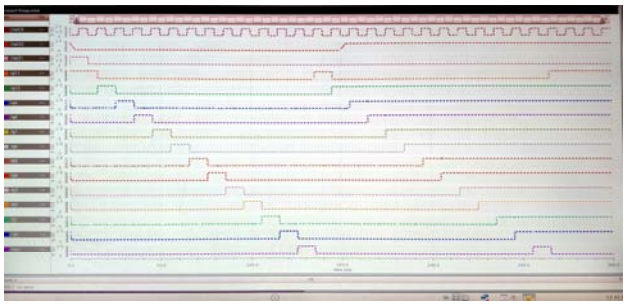

Fig 9 :SAR control logic output

Fig.9 shows the output of Successive Approximation Register control logic

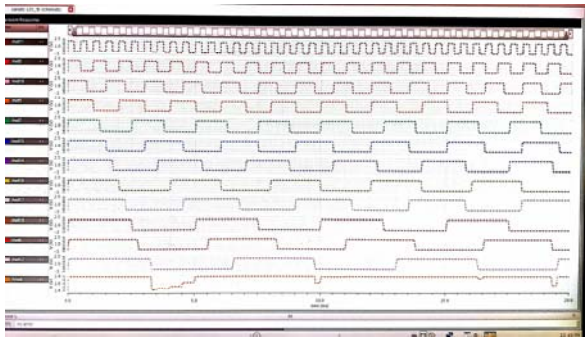

Fig.10:DAC simulation results

The output in fig.10 is the output of DAC which shows the conversion of digital signal into analog signal.

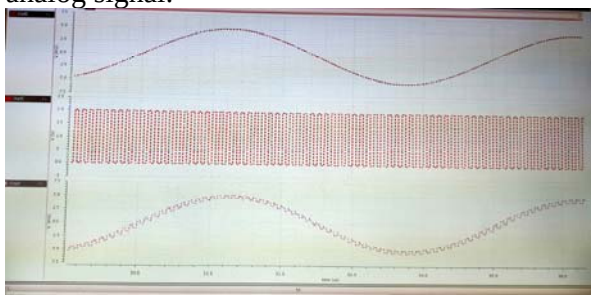

Fig 11: Sample and hold results

Fig.11 illustrates output waveform of sample and hold circuit.

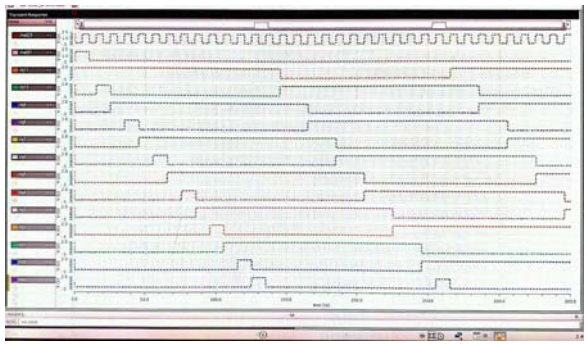

Fig 12 :SAR ADC simulation results

All the blocks are integrated to form the final ADC structure and is simulated on cadence. Fig.12 illustrates the conversion of analog signal to digital signal.

IV. CONCLUSION

In this design, C-2C DAC is used as it consumes less power and induces less mismatch errors when compared to resistive DAC. In order to increase the efficiency of ADC, improvised track and hold circuits can be used . This design can be further improvised by using less power consuming circuitry when compared to the one's being used in this paper.

V. REFERENCES

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