

## **4-BIT BARREL SHIFTER USING TRANSMISSION GATES**

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## Abstract

Barrel shifter plays an important role in the floating point arithmetic operations and optimizing the RISC processor and used for rotating andshifting the data either in left or right direction. This shifter is useful in many signal processing ICs. The arithmetic and logical shifter are itself a type of barrel shifter. The main objective of this paper is to design a fully custom two bit barrel shifter using 4x1 multiplexer with the help of transmission gates and analvze the performance on basis of power consumption, and no of transistors. The tool used to fulfill the purpose is cadence virtuoso using 180nm technology.

Keywords: Barrel shifter, Transmission gates, Multiplexer

## **I.INTRODUCTION**

Fundamentally there are four sorts of shifters i.e. consistent shifter, math shifter, barrel shifter and channel shifter. A barrel shifter is a combinational rationale hinder that will move the substance of a transport determined number of positions left or great by a control word. This is an imperative capacity in PCs and numerous sign preparing ICs. Regularly, when moving to one side, the positions cleared will be loaded with qualities from the left, or if no qualities are accessible, then loaded with zeros also when no qualities are accessible, the emptied positions might be filled the estimation of the most critical piece (MSB) [2]. A few shifters really turn the substance of a transport filling the slightest critical bits (LSBs) with the past substance of the MSBs for a shift left and the other way around for a shift right.

In Arithmetic shifter the procedure for left shifting is same as logical but in case of right shifting the empty spot is filled by signed bit. Funnel Shifter is combination of all shifters and rotator In this paper barrel shifter is designed using multiplexer and implemented using CMOS logic.The MUX used is made with the help of universal gates so that the time delay and power dissipation is reduced.

## **II. BARREL SHIFTER**

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits without the use of any sequential logic, only pure combinatorial logic. One way to implement it is as a sequence of multiplexers where the output of one multiplexer is connected to the input of the next multiplexer in a way that depends on the shift distance. A barrel shifter is often used to shift and rotate nbits in modern microprocessors, typically within a single clock cycle.

A common usage of a barrel shifter is in the hardware implementation of floating-point arithmetic. For a floating-point add or subtract operation, the significant of the two numbers must be aligned, which requires shifting the smaller number to the right, increasing its exponent, until it matches the exponent of the larger number. This is done by subtracting the exponents and using the barrel shifter to shift the smaller number to the right by the difference, in one cycle. If a simple shifter were used, shifting by n bit positions would require n clock cycles.

## **III. TRANSMISSION GATE**

A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously. Resistance characteristic of a transmission gate.

**Principle diagram of a transmission gate**. The control input ST must be able to take to control depending on the supply voltage and switching voltage different logic levels.

In principle, a transmission gate made up of two field-effect transistors, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal (bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a pchannel MOSFET, are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate (inverter), to form the control terminal.

Two variants of the "bow tie" symbol commonly used to represent a transmission gate in circuit diagrams

Unlike with discrete FETs, the substrate terminal is not connected to the source connection. Instead, the substrate terminals are connected to the respective supply potential in order to ensure that the parasitic substrate diode (between gate and substrate) is always reversely biased and so does not affect signal flow. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply potential, and the substrate terminal of the n-channel MOSFET connected to the negative supply potential.

Function

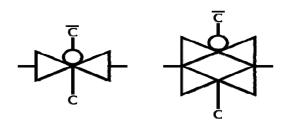
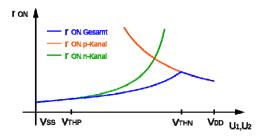


Figure 1: Schematic diagram of transmission gate



VTHN and VTHP denote those positions at which the voltage to be switched has reached a potential, where the threshold voltage of the respective transistor is reached.

When the control input is a logic zero (negative power supply potential), the gate of the nchannel MOSFET is also at a negative supply voltage potential. The gate terminal of the pchannel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off.

When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts.

One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain

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voltage) on the n-channel MOSFET, and this begins to turn off. At the same time, the pchannel MOSFET has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches.

Thereby it is achieved that the transmission gate passes over the entire voltage range. The transition resistance of the transmission gate varies depending upon the voltage to be switched, and corresponds to a superposition of the resistance curves of the two transistors.

## **IV.** Multiplexer

Multiplexers, or MUX's, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET's or relays to switch one of the voltage or current inputs through to a single output.

## **Basic Multiplexer**

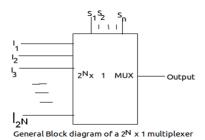


Figure 2: Basic block diagram of multiplexer

In digital electronics, multiplexers are also known as data selectors because they can "select" each input line, are constructed from individual Analogue Switches encased in a single IC package as opposed to the "mechanical" type selectors such as normal conventional switches and relays.

They are used as one method of reducing the number of logic gates required in a circuit design or when a single data line or data bus is required to carry two or more different digital signals. For example, a single 8-channel multiplexer.

Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called control lines and according to the binary condition of these control inputs, either "HIGH" or "LOW" the appropriate data input is connected directly to the output. Normally, a multiplexer has an even number of 2n data input lines and a number of "control" inputs that correspond with the number of data inputs.

We can build a simple 2-line to 1-line (2-to-1) multiplexer from basic logic NAND gates as shown.

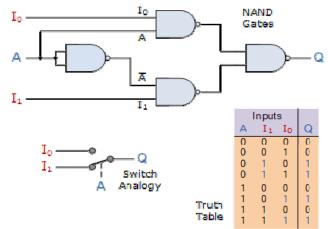


Figure 2.1: 2x11 mux using NAND gate

# **RTL Schematic of 4-bit Shifter Using Transmission Gates**

Barrel shifter is designed using mux symbol. It requires just 4, 4x1 multiplexers

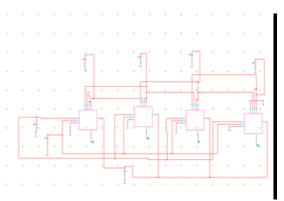


Figure 3: Block diagram of Barrel shifter **2x1 Multiplexer using transmission gate** 

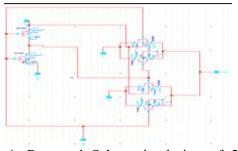


Figure 4: Proposed Schematic design of 2:1 MUX

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Proposed design of 2:1 MUX is shown in which transistor are placed using transistor logic. Thus the no of transistors is reduced. Therefore the power consumption and time delay is also reduced further in the design of barrel shifter.

## **Output Waveform Of 2X1 Multiplexer**

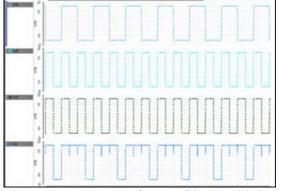


Figure 5: output waveforms of 2x1 multiplexer

In fig.5 two inputs A, B and one selection line(SEL)are taken, the value of A is 010101and so on and B is 1010101 and so on and SEL is 101010 and so on and the output(Y) is obtained according to 2X1 mux, thus when A is low, B is high and SEL is high the output Y is high. Similarly, when A,B both are high and SEL is low then Y is high. In the same way output waveform is obtained but with a little distortion and after analysis it can be concluded that distortion occurs in output at the time of change of values of inputs.

Fig.3 shows the waveform of 4-bit barrel shifter in which input is shifted/rotated to the right by one bit and output is obtained. The output is shown for two inputs, in the first one rotated by one bit and in the second input its is shifted by one bit.

## 4X1 Multiplexer Using 2X1 Multiplexers:

Below figure shows the implementation of 4x1 multiplexer uses the 2x1 multiplexers. To implement the 4x1 multiplexer it just requires the 3 number of 2x1 multiplexer only. Based on the selection lines output will be decided i.e., sel1 and sel2.

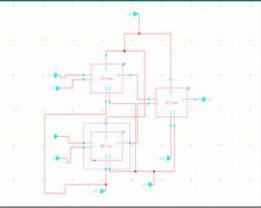


Figure6: 4x1 multiplexer using 2x1 multiplexer

## Final output of 4-bit barrel shifter:

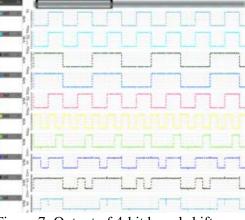


Figure 7: Output of 4-bit barrel shifter

The above figure will give the complete analysis of 4 bit barrel shifter. In the above figure blue and green are two selection lines i.e., s0, s1 respectively and also see the input and output from bottom to top. The truth table of the shifter is given below. In truth table for two set of selection lines i.e., 00, 01 there is no change in the output, that means same input will be reflected at output side. For 10 it is going to do right shift operation by inserting 0 in MSB bit. And also for 11 barrel shifter perform the left shift operation by pushing 0 in the LSB. It is explained clearly in the truth table.

The result & analysis of the barrel shifter is done in cadence virtuoso software. The schematic is constructed using 45nm technology. The transient response for the multiplexer and barrel shifter is obtained. The proposed designed schematic is compared with the conventional Barrel shifter made in the gpdk 180nm.

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Table 1:Truth table						
<b>S0</b>	<b>S1</b>	D3	D2	D1	D0	
0	Χ	A3	A2	A1	AO	
1	0	A2	A1	A0	0	
1	1	0	A3	A2	A1	

### **Table 2: The Performance of Barrel Shifter**

Parameter	Conventional	Proposed
	method	method
Power	77.85mw	17.76mW
consumption		
No of	216	72
Transistors		

## CONCLUSION

In this paper, two different MUX is designed one is using universal gates and other is using pass transistor logic, for one 4x1 mux gate design no of transistors used are 54 while in transmission gate logic the no of transistors used are 18.Thus the final circuit for barrel shifter using conventional design i.e. using universal gate, uses 216 transistors with more power consumption. On the other hand the proposed barrel shifter uses total 72 transistors with less power consumption. From table the percentage reduced can also be seen. Thus it can be concluded that proposed barrel shifter is better than conventional circuit.

## REFERENCES

- RenukaVerma, Rajesh Mehra, "Area Efficient Layout Design AnalysisOf CMOS Barrel Shifter," International Journal of Scientific Research Engineering & Technology (IJSRET), pp. 84-89, March 2015.
- [2]. A Sharma, Rajesh Mehra, "Area and Power Efficient CMOS Adder Design By Hybridizing PTL and GDI Technique," International Journal of Computer Applications, Vol.66, No.4, pp.15-22, March 2013.
- [3]. Shilpa Thakur, Rajesh Mehra, "CMOS Design and Single Supply Level Shifter Using 90nm Technology," Conference on

Advances in Communication and Control Systems, pp.150-153, 2013.

- [4]. R Singh, Rajesh Mehra, "Power Efficient design of Multiplexer using Adiabatic logic," International Journal Of Advances Engineering and Technology, Vol.6, Issue.1, pp.246-254, March 2013.
- [5]. Prasad DKhandekar, Dr. Mrs. ShailaSubbaraman, "Low Power 2:1 MUX for Barrel Shifter," International Conference On Emerging Trends In Engineering and Technology,IEEE, pp.404-407, July 2008.
- [6]. P.VamsiPriya, Anita Angeline.A, "Design of Variable Width Barrel Shifter for RISC Processor," International Journal Of Research in Electronics & Communication Technology(IASTER), Vol.1, Issue 2, pp. 7-11,December 2013.
- [7]. JyotiSankarSahoo, Nirmal Kumar Rout, Comparative Study on Low Power Barrel Shifter/Rotator at 45nm technology," International Journal Advanced of Engineering and Nano Technology(IJAENT), Vol.2 Issue 6, pp.11-18, May 2015.
- [8]. [8] Ravish Aradhya H.V, Lakshmesha J, Muralidhara K.N, "Design optimization of reversible Logic Universal Barrel Shifter for Low Power applications," International Journal Of Computer Applications, Vol 40, No.15, pp.26-34, February 2012.
- [9]. Prasad D Khandekar, ShailaSubbaraman and Venkat Raman Vinjamoori, "Quasi-Adiabatic 2X2 f Shifter," 4th International Conference On Industrial and Information Systems ICIIS-2009, 28-31 December 2009, pp.321-324.
- [10]. G.M.Tharakan, S.M.Kang, "A New Design of a fast Barrel Switch Network," IEEE Journal of Solid State Circuits, Vol.28, pp.217-221, February 1992.
- [11]. Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design", Pearson publications, 4th edition, pp.472-476.\