



DESIGN OF LOW POWER HIGH PERFORMANCE 4 -16 MIXED LOGIC LINE DECODER

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Abstract

A mixed-logic design method for line decoder, combining transmission gate logic, pass transistor for dual value logic and static complementary metal-oxide semiconductor (cmos), Two novel topologies are presented for the 2-4 decoder. A 14 transistor topology aiming on minimizing transistor count and power dissipation and a 15 transistor topology aiming on high power, delay performance. Normal decoder are implemented, yielding a total of two new designs. Furthermore new 4-16 decoders are designed by using 2-4 mixed logic predecoders. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally simulation is done by using Cadence at 180nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

Keywords: Mixed logic, decoder, CMOS logic, Transmission gate

I. INTRODUCTION

STATIC cmos circuits are used for the vast majority of logic gates in integrated circuits. They consist of complementary N-type metal-oxide-semiconductor (nMOS) pulldown and P-type metal-oxide semiconductor (pMOS) pullup networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input

signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors.

Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM) . This brief develops a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design.

A	B	D ₀	D ₁	D ₂	D ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TABLE I

TRUTH TABLE OF THE 2-4 DECODER

The rest of this brief is organized as follows: Section II provides a brief overview of the examined decoder circuits, implemented with conventional CMOS logic. Section III introduces the new mixed-logic designs. Section IV conducts a comparative simulation study among the proposed and conventional decoders, with a detailed discussion on the derived results.

Section V provides the summary and final conclusions of the work presented.

II. OVERVIEW OF LINE DECODER CIRCUITS

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate the m = 2n minterms of n input variables.

A. 2-4 Line Decoder

A 2-4 line decoder generates the 4 minterms D0-3 of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2-4 decoder generates the complementary minterms I0-3, thus the selected output is set to 0 and the rest are set to 1. In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2-4 decoder can be implemented with 2 inverters and 4 NOR gates, whereas an inverting decoder requires 2 inverters and 4 NAND gates, both yielding 20 transistors.

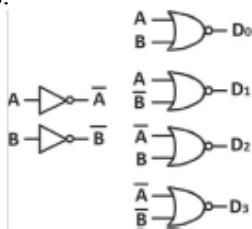


Fig. 1. 20-transistor 2-4 line decoders implemented with CMOS logic.

B. 4-16 Line Decoder

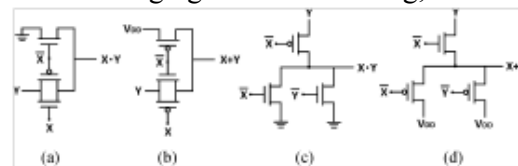
With 2-4 Predecoders A 4-16 line decoder generates the 16 minterms D0-15 of 4 input variables A, B, C, and D, and an inverting 4-16 line decoder generates the complementary minterms I0-15. Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder.

Therefore, a 4-16 decoder can be implemented with 2 2-4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2-4 decoders and 16 2-input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

III. NEW MIXED-LOGIC DESIGNS

Transmission gate logic (TGL) can efficiently implement AND/OR gates, thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown respectively. They are full-swinging, but not restoring for all input combinations.

Regarding PTL, there are two main circuit styles: those that use nMOS-only pass transistor circuits, like CPL [3], and those that use both nMOS and pMOS pass transistors, like DPL and DVL. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count. The 2-input DVL AND/OR gates, respectively. They are fullswinging but non-restoring, as well.



Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL AND gate. (d) DVL OR gate.

Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. We labeled the 2 gate inputs X and Y. In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y as the control signal and propagate signal of the gate, respectively. Using a complementary input as the propagate signal is not a good practice, since the inverter

added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A B) or implication (A + B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A + B) function, either choice is equally efficient. Finally, when implementing the NAND (A + B) or NOR (A B) function, either choice results to a complementary propagate signal, perforce.

A. 14-Transistor 2-4 Low-Power Topology

Designing a 2-4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14.

Let us assume that, out of the two inputs, namely, A and B, we aim to eliminate the B inverter from the circuit. The D0 minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. The D1 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. The D2 minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. Finally, The D3 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. These particular choices completely avert the use of the complementary B signal therefore, the B inverter can be eliminated from the circuit, resulting in a 14-transistor topology (9 nMOS and 5 pMOS).

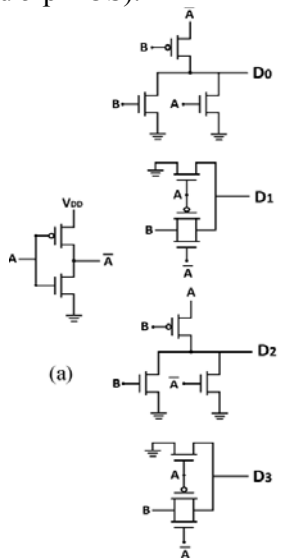


Fig. 4. New 14-transistor 2-4 line decoders. C. Integration in 4-16 Line Decoders

Following a similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: I0 and I2 are implemented with TGL (using B as the propagate signal), and I1 and I3 are implemented with DVL (using A as the propagate signal). The B inverter can once again be elided.

Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named “2-4LP” and “2-4LPI,” where “LP” stands for “low power” and “I” for “inverting.”

15-Transistor 2-4 High-Performance Topology

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, D0 and I3 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation. They are named “2-4HP” (9 nMOS, 6 pMOS) and “2-4HPI” (6 nMOS, 9 pMOS), where “HP” stands for “high performance” and “I” stands for “inverting.”

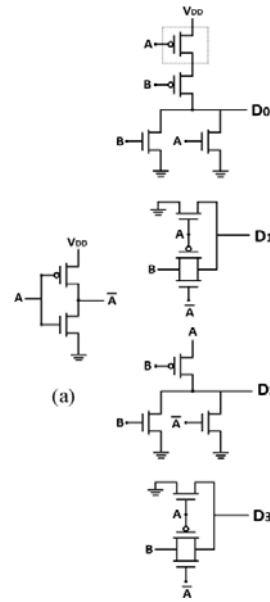


Fig. 5. New 15-transistor 2-4 line decoders.

PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed-topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results.

We implemented four 4–16 decoders by using the four new 2–4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are the following: 4–16LP which combines two 2–4LPI predecoders with a NOR-based postdecoder; 4–16HP [Fig. 6(b)], which combines two 2–4HPI predecoders with a NOR-based postdecoder; 4–16LPI [Fig. 6(c)], which combines two 2–4LP predecoders with a NAND-based postdecoder; and, finally, 4–16HPI which combines two 2–4HP predecoders with a NAND-based postdecoder. The “LP” topologies have a total of 92 transistors, while the “HP” ones have 94, as opposed to 104 with pure CMOS.

IV. SIMULATIONS

In this section, we perform a variety of BSIM4-based spice simulations on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional CMOS. The circuits are implemented using a 32 nm predictive technology model for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect [11]. For fair and unbiased comparison we use unit-size transistors exclusively ($L_n = L_p = 32$ nm, $W_n = W_p = 64$ nm) for all decoders.

A. Simulation

Setup All circuits are simulated with varying frequency (0.5, 1.0, 2.0 GHz) and voltage (0.8, 1.0, 1.2 V), for a total of 9 simulations. Each simulation is repeated 5 times with varying temperature (-50 , -25 , 0 , 25 , and 50 °C) and the average power/delay is calculated and presented in each case. All inputs are buffered



Fig:6 Simulation Results a) 2-4 Decoder, b) 4-16 Decoder

with balanced inverters ($L_n = L_p = 32$ nm, $W_n = 64$ nm, $W_p = 128$ nm) and all outputs are loaded with a capacitance of 0.2 fF. Furthermore, proper bit sequences are inserted to the inputs, in order to cover all possible transitions a decoder can perform. A 2–4 decoder has 2 inputs, which can generate $2^2 = 4$ different binary combinations, thus yielding a total of $4 * 4 = 16$ possible transitions. The 2–4 decoders are simulated for 64 nanoseconds (ns), so that the 16-bit input sequences are repeated 4 times. Similarly, a 4–16 decoder has 4 inputs, $2^4 = 16$ input combinations and $16 * 16 = 256$ possible transitions, therefore the 4–16 decoders are simulated for 256 ns to exactly cover all transitions once. Fig. 8 depicts the input/output waveforms of our proposed 2–4 decoders for all 16 input transitions, demonstrating their full swinging capability.

B. Performance

Metrics Examined The metrics considered for the comparison are: average power dissipation, worst-case delay and power-delay product (PDP). With continuous sub-micron scaling and low voltage operation, leakage power has become increasingly important as it dominates the dynamic one [12]. In our analysis, both leakage and active currents are considered and

the total power dissipation is extracted from spice simulation, measured in nanowatts (nW). Regarding delay, we note the highest value that occurs among all I/O transitions, measured in picoseconds (ps). Finally, PDP is evaluated as average power*max delay and measured in electronvolts (eV).

C. Result Discussion

The simulation results regarding power, PDP and delay are shown in Tables III–V, respectively. Each of the proposed designs will be compared to its conventional counterpart. Specifically, 2–4LP and 2–4HP are compared to 20T, 2–4LPI and 2–4HPI are compared to inverting 20T, 4–16LP and 4–16HP are compared to 104T and finally, 4–16LPI and 4–16HPI are compared to inverting 104T.

According to the obtained results, 2–4LP presents 9.3% less power dissipation than CMOS 20T, while introducing a cost of 26.7% higher delay and 15.7% higher PDP. On the other hand, 2–4HP outperforms CMOS 20T in all aspects, reducing power, delay, and PDP by 8.2%, 4.3%, and 15.7%, respectively. Both of our inverting designs, 2–4LPI and 2–4HPI, outperform CMOS 20T inverting in all aspects as well. Specifically, 2–4LPI reduces power, delay, and PDP by 13.3%, 11%, and 25%, respectively, while 2–4HPI does so by 11.2%, 13.2%, and 25.7%.

	time (s)	VT("/vd...") (V)
1	0.000	41.78E-9
2	312.5E-9	41.78E-9
3	733.3E-9	41.78E-9
4	943.6E-9	41.78E-9
5	1.049E-6	41.78E-9

	time (s)	VT("/vd...") (V)
1	0.000	108.5E-6
2	621.5E-15	108.5E-6
3	1.225E-12	108.5E-6
4	2.433E-12	108.5E-6
5	4.849E-12	108.5E-6
6	7.424E-12	108.5E-6

Fig: 7 Power and Delay a) Milli watts b) Nano watts

Regarding the 4–16 simulations, the obtained results are similar. The 4–16LPI decoder, presents 6.4% lower power dissipation with the cost of 17.9% higher delay and 1.9% higher PDP than CMOS 104T. The rest of the decoders, namely, 4–16LP, 4–16HP, and 4–16HPI, present better results than corresponding CMOS decoders in all cases, which can be

summarized as follows: 7.4%, 6.5%, and 6.0% lower power; 4.5%, 9.3%, and 2.3% lower delay; and 11.1%, 15.3%, and 7.9% lower PDP, respectively.

V. CONCLUSION

This brief has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved powerdelay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits, combined with postdecoders implemented in static CMOS to provide driving capability.

A variety of comparative spice simulations was performed at 32 nm, verifying, in most cases, a definite advantage in favor of the proposed designs. The 2–4LP and 4–16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2–4LPI, 2–4HP, and 2–4HPI, as well as the corresponding 4–16 topologies (4–16LP, 4–16HPI, and 4–16HP), proved to be viable and all-around efficient designs; thus, they can effectively be used as building blocks in the design of larger decoders, multiplexers, and other combinational circuits of varying performance requirements.

Moreover, the presented reduced transistor count and lowpower characteristics can benefit both bulk CMOS and SOI designs as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

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