OPTIMIZATION OF ACTIVE POWER AND DELAY OF 1-BIT FULL ADDER AT 40NM TECHNOLOGY

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Abstract:

The performance analysis and compression between various parameters of a low power high speed conventional 1-bit full adder has been presented here. The work elucidated here gives a quantitative comparison of the adder cell performance. This paper shows the advancement over active power, leakage current and delay. The comparative study based on a new logic approach, which reduces power consumption. With power supply of 0.7V, we have achieved reduction in active power consumption of 98.28nW and propagation delay of 0.737ns, which makes this circuit highly energy efficient. In this circuit we have reduced leakage current of 135.9nA. The designs have been carried out by virtuoso tool of cadence at 45nm technology.

Index Terms- Full adder,low power, CMOS circuits, logic devices, performance.

I. INTRODUCTION

ower minimization is one of the primary concerns in today's VLSI design methodologies because of two reasons one is the long battery operating life requirement of portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation. In VLSI applications, 1-bit full adder cell is the fundamental gate used in many arithmetic circuits like adders and multipliers. Thus, increasing the performance of the full adder block leads to the enhancement of the overall system performance

[1] [2]. Therefore, many efforts have been made to implement high-speed and low power 1-bit full adder cells with smaller area [3] [4]. A full adder has three inputs and two outputs block in which the outputs are compressors and comparators are full adders [5]. There are several issues related to the full adders. Some of them are performance, power dissipation, area, regularity, noise immunity and good driving ability [6].

the addition of three inputs. Basic fundamental units used in various circuits such as parity checkers,

This technology is used with increasing demand for battery-operated portable applications such as cell phones, laptop computers, PDAs etc. as well as low intensity applications such as distributed sensor network in which power sensitive design has grown significantly. Today's, there are an ever increasing number of portable applications requiring low power and high throughput circuits. Hence low-power design has become a major design consideration [7] [8] [9]. It has been shown that reducing the supply voltage is the most direct means of reducing dissipated Power [10] [11] and operating CMOS devices in the sub-threshold region is considered to be the most energy-efficient solution for low-performance applications. The aim of this study is to design 1-bit low power, minimum delay full adder cell, based on a new logic approach without losing driving capability. Power and delay are the premium resources for designers. They always try to save when designing a system.

II. REVIEW OF FULL-ADDER DESIGN

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A 1-bit full adder adds three one bit numbers, often written as A, B and C. A and B are the operands and C is a bit carried in from the next less significant stage. Full adder is usually a component in a cascade of adders, which add 8, 16, 32, 64 etc. binary numbers. The circuit generates a two-bit output sum typically represented by the signals Carry and Sum. Here a full adder is constructed with the help of two half adders by connecting A and B to the input of first half adder, connecting the sum from that to an input to the second adder, connecting C to the other input and OR the two carry outputs. Similarly, Sum could be made the three bit XOR of A, B, and C, and Carry could be made the three-bit majority function of A, B, and C .

The expression of Sum and Carry outputs of 1-bit full a adder based on binary inputs A, B, C are represented as:

$$Sum = A \oplus B \oplus C \quad \ldots\ldots\ldots\ldots (1)$$

$$Carry = AB + BC + CA \quad \ldots\ldots\ldots\ldots\ldots (2)$$

$$Sum\ Carry = (A \oplus B) \oplus C \quad \ldots\ldots\ldots (3)$$

TABLE I

TRUTH TABLE OF FULL ADDE

Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

III. CONVENTIONAL CMOS FULL-ADDER

The 1-bit conventional CMOS full adder cell is one of the well-known logic style used to implement different functions. The CMOS structure combines PMOS (pull-up network) and NMOS (pull-down network) to produce considered outputs. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, each may be consist of several sub-branches. Figure 3 shows the conventional CMOS 28 transistor adder. A basic cell digital computing system is the 1-bit full adder which has three 1-bit inputs (A, B and C) and two 1-bit outputs (Sum and Carry). The relationship between the inputs and the outputs are represented as:

‘’’’’’

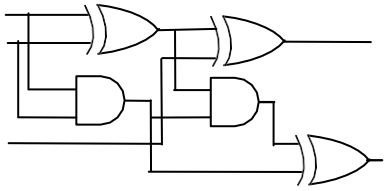

Figure 2. Schematic of a full adder.

The above Boolean expressions may be rearranged as:

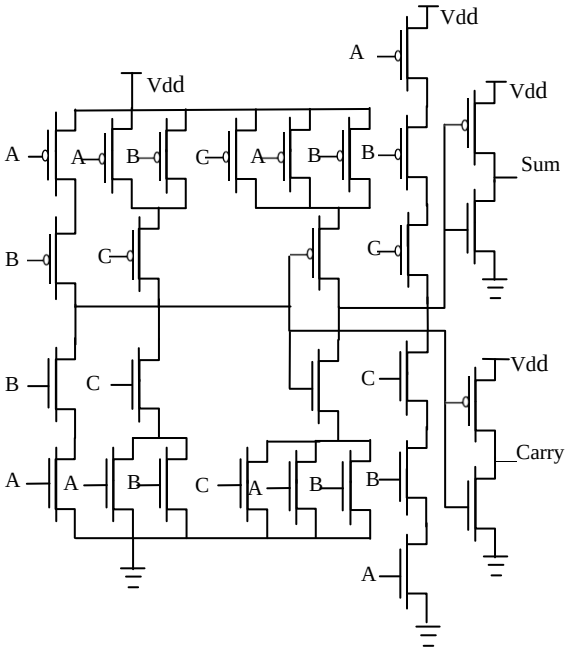

Figure 3. Schematic of Conventional CMOS full adder

An easy way to comply with the conference paper fo The CMOS design style is not area efficient for complex gates with large fan in. So that care must be taken when a static logic style is selected to realize a logic function. Pseudo NMOS techniques are used to compromise noise margin and suffers from static power dissipation. Charge leakage is frequently used for reducing the operational frequency of the circuit.

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IV. POWER CONSUMPTION IN CONVENTIONAL CMOS FULL-ADDER

The average power consumption in a generic digital CMOS gate is given as [12]:

Where fclk is the system clock frequency, Viswing is the voltage swing at node i, Ciload is the load Capacitance at node i, αi is the activity factor, Iisc is the short circuit current and Iisc is the leakage current. Generally CMOS devices in the subthreshold region, the power supply voltage is always kept lower than the device threshold voltage. This conforms that the

transistor channel is never fully inverted, but is accomplished in weak or moderate inversion while the transistor is in its 'on' state. Due to the exponential V-I relationship, sub-threshold logic gates have a near ideal voltage transfer characteristics [13]. The V-I relation of the saturated device in weak inversion through the EKV model is expressed as [14] [15].

V. SIMULATION AND ANALYSIS

We have performed the simulated results using spectre simulator of cadence tool. The supply voltages are 0.7V (45nm) and 1.8v (180nm). The data analysis of the input and output such as A, B, C, sum and carry shown in figure 4. The output waveform of 1-bit full adder simulated under the process of transient analysis at 45nm technology. Here the simulated waveform is of period 100ns and power supply 0.7V.

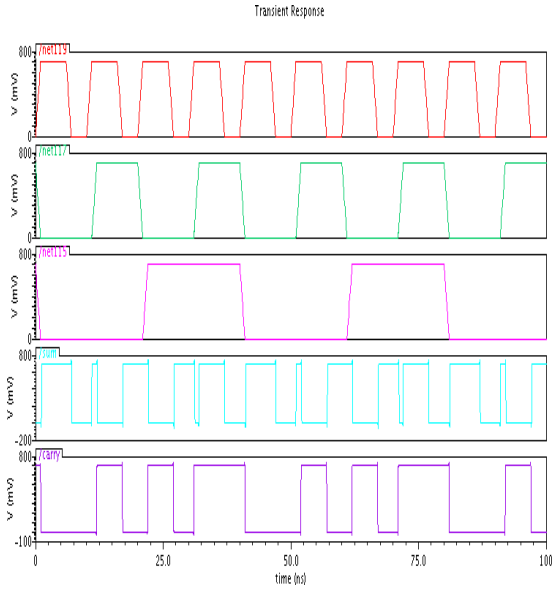

Figure 4. Simulated output waveform of transient response at 45nm technology.

Figure 5 shows the output waveform of leakage power consumption of 95.13 nW of full adder simulated at 45nm technology with the power supply of 0.7V. This power consumption is divided between active power (Pactive ≈ CV2 f) which is the power used while the product is performing its various function and leakage power Pleakage ≈ 1V, which is the power consumed by unintended leakage that does not contributed to the IC's function.

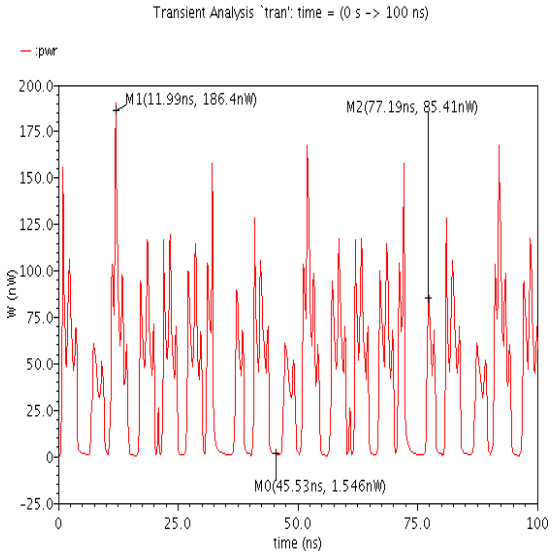

Figure 5. Simulated output waveform of leakage power at 45nm technology.

Figure 6 shows the output waveform of leakage current of 1-bit full adder simulated under the process of transient analysis at 45nm technology. Here the simulated waveform is of period 100ns and power supply 0.7V. Leakage current is also the current that flow when the ideal current is zero, such as in electronic assemblies that are in stand by disabled or "sleep" mode.

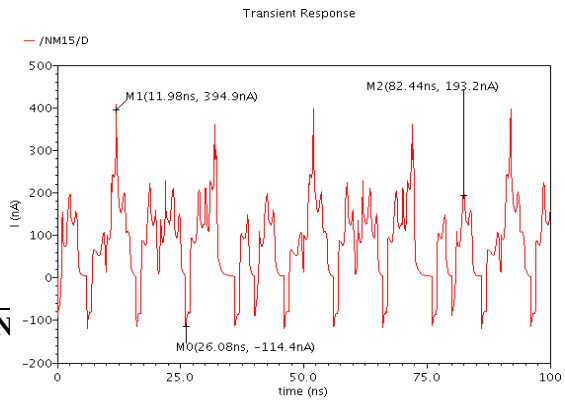

Figure 6. Simulated output waveform of leakage current at 45nm technology.

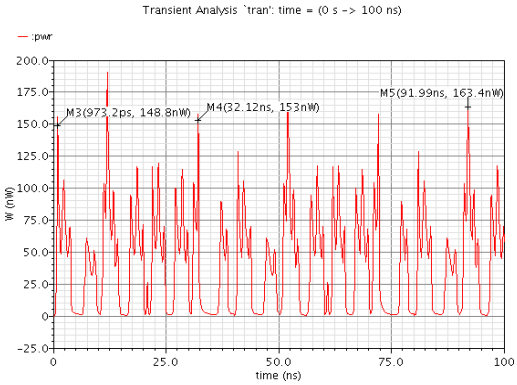

Figure 7. Simulated output waveform of active power at 45nm technology

Figure 7 shows the output waveform of active power simulated under the process of transient analysis at 45nm technology. Here the simulated waveform is of period 100ns and power supply 0.7V.

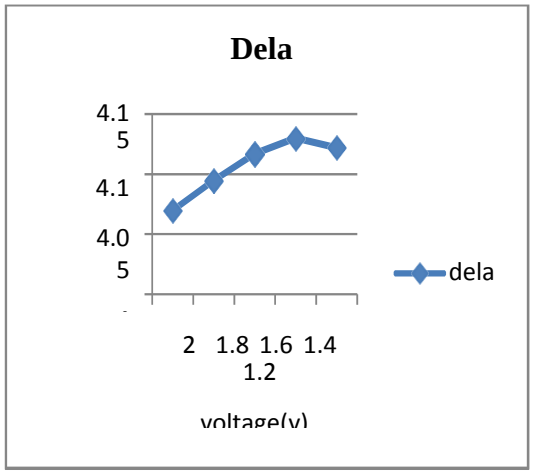

Figure 8. Delay of conventional CMOS full adder at 180nm technology

VI. CONCLUSION

Simulation of full adder has been done at 45nm technology for calculation of different parameters and is compared with the full adder simulation results at 180nm technology. The results signify that power consumption of the circuit is reduced to 98.2nW for 0.7V at 45nm and reduces further on reduction of the supply voltage. Delay has also been improved and reduced to 0.737 ns at 0.7V at 45nm technology. The comparison shows that the implementation of the full adder would be better at 45nm technology as compared to 180nm.

VII. ACKNOWLEDGMENT

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