IMPLEMENTATION OF AND, OR & NOT LOGICAL OPERATION USING MULTIPLEXER

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Abstract
As the receiving end of an optical network opto electronics conversion of data takes place for the processing purpose. Electronic processing of high speed data dissipates huge amount of heat energy. This heat is directly proportional to the elements which are used in any circuit. Huge numbers are elements used in any circuit design it means no huge amount of heat dissipation. This problem can be solved by reducing the number of element in the same circuit. In this proposed model the above said problem can be reduced.
Keywords: Multiplexers (mux); Optical logic gate; AND, OR, NOT.

I.INTRODUCTION

In the present society where we live is full of digital equipments wherever we see, as we are living and experiencing the information era. In today's world huge amount of data is being generated, transported and processed. Optical fiber is the medium used for transportation of data at very high rate. For electronics processing, opto-electronic conversion of data takes place at the receiving end high data rate signal processing result in increased consumption of power and heat generation from electronic integrated circuit. It is stated in few papers (notomi et al.2011)[1]; Shancham et al.(2008)[2] that even the electronic transportation of high speed data among the processing nodes consumes major chunk of energy. These are the limiting factors in expanding high speed data networking and processing. If data is being transported in optical domain it should also be processed in optical domain and hence the elimination of opto electronic conversion and development of all optical processing is need of the hour. The main advantage of all optical data processing is its high data rate, low power consumption and fast dynamics. Optical logic gates are building blocks of the photonic processing circuits. In recent years extensive research has been done in designing of all optical logic gates like AND (Li et. Al. 2009)[3] OR(Singh et al. 2014)[4], NOT (Singh et al. 2013)[5], NAND (Mohammadnejad et. Al. 2009) [6] and NOR (Hamie et. Al. 2002) [7]. But all of the them used near about similar design to implement and no one try to reduced the circuit elements. In the proposed model we used multiplexer to design the logic gate (AND, OR & NOT). In the current paper a novel design of 3 basic logical operations.
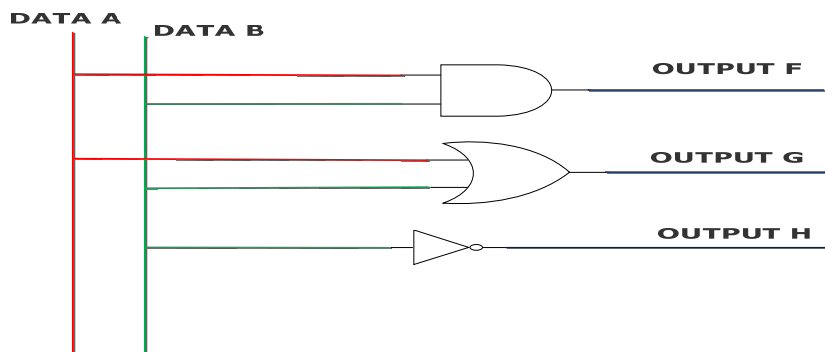

Fig. 1 Symbolic diagram of AND, OR and NOT gates

AND, OR and NOT which will save space if incorporated in more complex circuits. And also reduced the problem of heat dissipation, because more heat dissipation can harm the integrated circuit. A multiplexer is a kind of digital circuit having n input and one output known as n:1 multiplexer, also known as many to one circuit. It has 2^n- input mux has n select lines. Fig 1 shows the basic symbolic diagram of the proposed model.

II.PRINCIPLE OF OPERATION AND MODEL FORMULATION

In the proposed model the logical operation AND, OR and NOT are achieved with the help of Multiplexer. The red line shows the input data A while the representation of data B is by green colour other than these two input A ,B data all zero and All one are shows by Input data 0 and input data 1 respectively. In fig 2 the block diagram of proposed model is designed here data B is given in select line of multiplexer and input 0 is given as first input of multiplexer and input A given to second input of multiplexer output comes from here gives $A.B$ which is output of AND gate i.e output F. while in other hand input data A is given to Mux2 in first arm and input 1 in second arm of mux 2 and B as select line . the output comes from Mux2 is A+B i.e output of OR gate. Similarly in mux three data A as select line Input 1 and input 0 is given as input for mux 3 arms respectively. Here comes $\bar{A}$ as output.
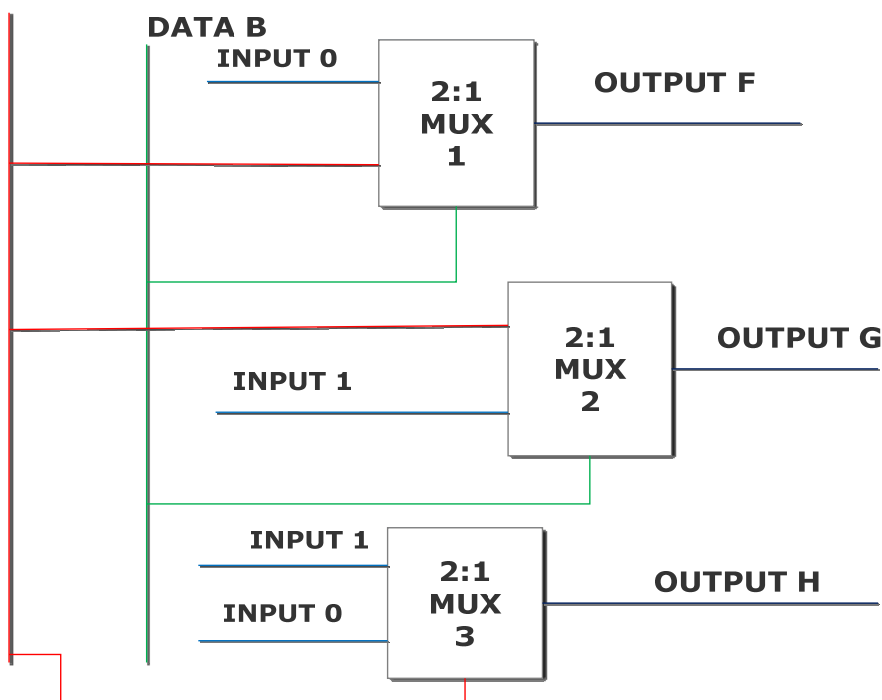

Fig. 2 block diagram of proposed model

TABLE 1. FUNCTIONAL TABLE FOR AND GATE

Serial no.	INPUT DATA A	INPUT DATA B	OUTPUT F=A.B
1.	0	0	0
2.	0	1	0
3.	1	0	0
4.	1	1	1

TABLE 2. FUNCTIONAL TABLE FOR OR GATE

Serial no.	INPUT DATA A	INPUT DATA B	OUTPUT G=$A+B$
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	1

TABLE 3. FUNCTIONAL TABLE FOR NOT GATE

Serial no	Input data A	Output H
1.	0	1
2.	1	0

III.A FORMULATION

Here A and B are inputs having data values (0011) and (0101) respectively

When data B is given as select lines of MUX 1. The mux process is described as follow.

RESULT FROM MUX 1 = 0x$\bar{B}$+ AxB

$$F = A.B$$

Above output F verified by standard result

For mux 2 one arm is inputed by data input A while in second arm the input is 1. The process of mux 2is described as follow

$$G = Ax\bar{B}+1xB$$
$$G = (A+B)(\bar{B}+B)$$
$$G = A+B$$

Above output **Q** verified By standard result of Output of OR gate.

For mux 3 the process described below

$$H = 1x\bar{A}+0xA$$
$$H = \bar{A}$$

IV.THEORITICAL

ANALYSIS

The Refractive index of the active region of a SOA is determined by the carrier density N of SOA, so pump signal propagating through the active region of SOA decreases its carrier density [8] and modulates the refractive index which in turn gives rise to phase modulation of the probe beam. Similarly XGM also takes place due to gain saturation of SOA. The dynamics of SOA are:

$$\frac{dN}{dt}=\frac{J}{ed}-R(N)-V_g.g(N).N_{ph} \qquad ----(1)$$

$$G(N)=\frac{L\sigma_g}{V}(N-N_0) \qquad ----(2)$$

Where N is the carrier density , J is the injection current density, R(N) is the recombination rate,

V_g is the group velocity of light , g(N) is the material gain coefficient, N_{ph} is photon density, e is the electron charge, d is the active layer thickness and N_{ph} is photon density. Γ is the confinement factor σ_g is the differential gain, V is the volume of the active region of SOA and N_0 is the carrier density for transparency. Gain per unit length of SOA is written as:

$$G =\Gamma.g(N)–\alpha \qquad ----- (3)$$

where α is the total loss coefficient per unit length. The overall gain for entire length of SOA increases exponentially and is described as:

$$G_s = e^{g.L} \qquad ------------(4)$$

Where L is the length of the active region of SOA.

IV. Result and discussion

The proposed design of photonic circuit works at 10 Gbps data rate. All three Mux's used in this design have similar values Fig. 3a-b represents the input signals, and the output signals represented by fig. 3c ,3d and 3e. F is the output of AND gate and it is verified by truth table Table1. Fig. 3c shows the output signal F. Fig 3d shows the output of OR for the Input A and Input value B and verified by the truth table of OR gate which is presented by table 2. The output comes from Mux3 is H which is verified by the truth table 3. The output signals shown here are actually the low power probe signals which are the inverted copy of their high power pump signals after passing through SOA. Therefore these overshoots occur for the rising edge of the high power pump signal which corresponds to falling edge of probe signal for the same instance of time. Both

rising edge of the pump signal as well as the falling edge of the probe signal experiences high gain due to the presence of high population of carriers for that period of time. One of the reasons for high population of carrier for that particular time period is the absence of high power pump signal just before the overshoot. The overshoot is actually instigated by the high power signal
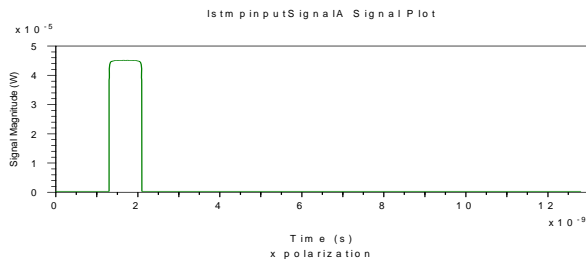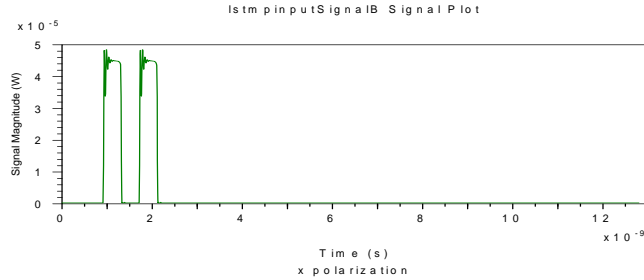

Fig.3(a) INPUT SIGNAL A
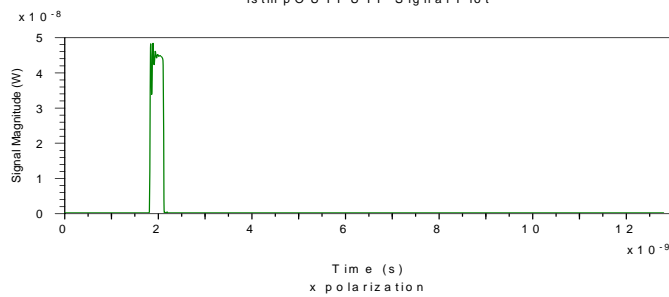

Fig.3(b) INPUT SIGNAL B
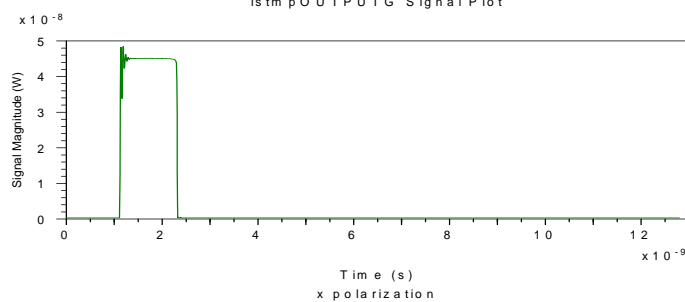

Fig.3(c) OUTPUT SIGNAL F (A.B)
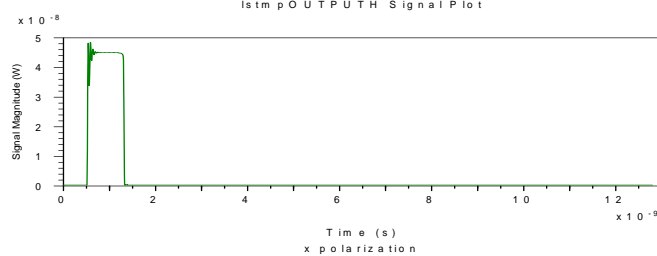

Fig.3(d) OUTPUT SIGNAL G (A+B)

Fig.3(e) OUTPUT OF NOT GATE

To evaluate the performance of the incorporated logic gates the extinction ratio and the quality factor for various lengths of active region of SOA and confinement factor of SOA are plotted. Extinction ratio is the ratio of two optical powers, power of bit 1 to the power of bit 0. For an efficient optical system the power gap between 1 and 0 should be large enough to facilitate the correct identification of the obtained bit. Therefore higher value of ER denotes better system performance. Extinction ratio is defined as the ratio of minimum output peak power of bit 1 to the maximum peak output power of bit 0 (Chattopadhyay 2011)[11].

V. Conclusion

An implementation of AND, OR and NOT optical gates in a single photonic circuit is done success-fully in this manuscript. Multiple optical gates onto a single chip will lead to optical signal processing in the future and electronic circuitry will be replaced by the optical circuitry. With the development of photonic circuitry it is now possible to get any digital result in optical domain. The very basic two input one output optical line selector can be integrated to form a part of more bigger and complex photonic circuit. Development of photonic circuits like these are leading towards all optical signal processing which is the ultimate goal.

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