

QUANTUM DOT CELLULAR AUTOMATION(QCA) BASED SEQUENTIAL CIRCUIT DESIGN

R.Indirapriyadharshini¹, G.Kalanandhini², D.Shankari³ ^{1,2,3}Assistant Professor,

Department of Electronics and Communication Engineering, Prince Shri Venkateshwara Padmavathy Engineering College, Chennai

ABSTRACT

Quantum dot cellular automation (QCA) is one of the emerging technology to design ultra-low-power and very high speed digital circuits. It is used for several binary and decimal arithmetic circuits. A quantum dot is a nanometer sized structure that is capable of trapping electrons in three dimensions. Ouantum dots are made by creating a conductive material surrounded by insulating material. Electrons that enter the quantum dot will be confined because of the high potential required to escape. Exploiting various proposed design OCA modules results in a computational speed higher than the existing design. It can be achieved by reducing the cell count and the latency. Keywords: QCA, SISO, SIPO, Polarization

I.INTRODUCTION

It is assumed that a system/circuit should function perfectly to provide accurate results in conventional digital VLSI design, Quantum-dot cellular automata (QCA) [1] technology has become one of the most attractive approaches for the development of next generation ultradense low-power high performance digital circuits. Quantum dots are nanostructures created from standard semi conductive material. The structures are modeled as quantum wells. They exhibited energy effects even at distances several hundred times larger than the material system lattice constant. A dot can be visualised as well. The basic building block of QCA is QCA cell which is created with four quantum dots placed at the corner of the cell. The electrons are forced into the quantum dots by electrostatic repulsion. The

electron in the cell that are placed adjacent to each other will interact, as a result the polarization of one cell will be directly affected by the polarization of its neighbouring cells. Fig 1(a) represents the cell and 1(b) represents the cell of +1 polarization(binary 0) and 1(c) represents the cell of -1 polarization(binary 0).

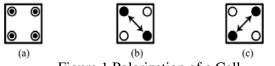
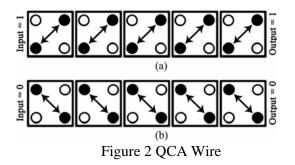


Figure 1 Polarization of a Cell The polarization of the cell can be changed by the utilization of the clock signal.

A.QCA WIRE

A QCA wire is needed to transmit signals. The wire consists of chain of cells and the binary information is transmitted based on the coulombic interaction. Since the polarization of each cell tends to align with that of its neighbours, a linear arrangements of standard cells can be used to transmit binary information from one point to another. The propagation in a 90 degree QCA wire is shown in Fig 2(a) and 45 degree QCA wire is shown in Fig 2(b).In this case the propagation of the binary signals alternates between the polarization.



B.QCA INVERTER

Two cells are placed in a diagonal fashion so the corner of the cell gets touched with each other. In order to avoid the repulsion the polarization of the cells gets modified. This type of behaviour can be used in designing a QCA inverter. The QCA inverter is shown in Fig. 3.Inverter of the two cells is shown in Fig. 4

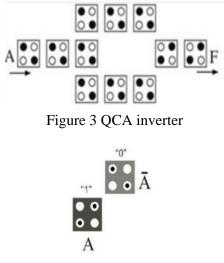


Figure 4 Two cell inverter

III.SEQUENTIAL CIRCUIT DESIGN

A sequential logic design involves both the present and past input values in order to compute the output.

A.SERIAL-IN PARALLEL-OUT SHIFT REGISTER

A serial -in/parallel-out shift register shifts data into internal storage elements and shifts data out at the serial-out, data-out pin. If the data bits are shifted by four clocks, the data becomes available on the four outputs QA to QD. The layout of SIPO is shown in Fig 5(a) and its simulation is shown in Fig 5(b).



Figure 5(a) Layout of SISO

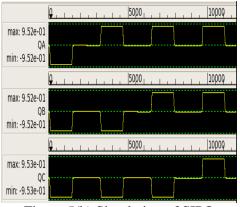


Figure 5(b) Simulation of SIPO

B.SERIAL-IN/SERIAL-OUT SHIFT REGISTER:

This type of shift registers accepts data serially, i.e. 1 bit at a time on a single input time. It displays the stored information in the serial form. Delay data by one clock time for each stage. It will store a bit of data for each register. The layout of SISO as shown in Fig 6(a) and its simulation is shown in Fig 6(b).

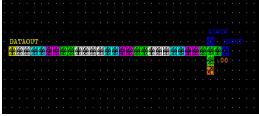


Figure 6(a) Layout of SISO

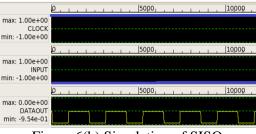


Figure 6(b) Simulation of SISO

B.DECODER:

The decoder allows N-inputs and generates 2 power N-numbers of outputs. The decoders play an essential role in digital electronics project. They are used to convert data from one form to another form. These are frequently used in communication system such as telecommunication, networking etc. to transfer data from one end to the other end. The layout of decoder is shown in fig.7

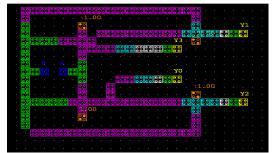


Figure7. Simulation of Decoder

IV.CONCLUSION

QCA technology is one of the promising nanotechnology in future can be used to build quantum computers.QCA sequential algorithm can be used to construct arithmetic logic units and microprocessors etc. The simulation decoder, SISO and SIPO have done using majority voting scheme.

REFERENCES

1. Cho and Swartzlander Jr E.E. (2007) "Adder Design and Analyses for Quantum- Dot Cellular Automata", IEEE Transactions on Nanotechnology, Vol.6, n°3,pp.374-383.

2. Gladshtein.M. (2011) "Quantum-Dot Cellular Automata Serial Decimal Adder",IEEE Transactions on Nanotechnology, Vol.10, n°6, pp.1377-1382.

3. Han.L. and Ko.S.B. (2013) "High-Speed Parallel Decimal Multiplication with Redundant Internal Encodings", IEEE Transactions on Computers, Vol.62, n°5, pp.956-968, 2013.

4. Kenney.R.D and Schulte M.J.(2005) "High-Speed Multioperand Decimal Adders", IEEE Transactions on Computers, Vol.54, n°8, pp.953-963, 2005.

5. Perri.S and Corsonello P.(2014) "Area-Delay Efficient Binary Adders in QCA", IEEE Transactions on VLSI Systems, Vol.22, n°5, pp.1174-1179,