LEAKAGE REDUCTION BY MULTI-GATE CMOS DESIGN

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Abstract—Scaling is the prime thrust for development of CMOS circuits, which increases in the number of faults and leakage current in manometer scale in ultra-low power circuit design. FinFET is the popular method to suppress the shorter channel effect and controls the leakage current. In this Paper we have analyse the behaviour of FinFET technology in digital circuit design and measure all the electrical characteristics for developments of EDA tool and Projects in different gates and benchmark circuit at different temperature. In this paper we examine the behaviour of different gate by using FinFET technology by using SP and LP mode of FinFET.

Index Terms—FinFET, Power consumption, PDP, Multigate and Fins.

I. INTRODUCTION

As device size reduces to increase the integration of digital circuit in conventional MOSFET has been mitigated significantly in last decade. With the dramatic increase in chip complexity ULSI (Ultra Large Scale Integration), number of transistors and power consumption are growing rapidly. Nano technology trends show that circuit propagation delay is scaling down by 30%, transistor density doubled and the transistor's threshold voltage (V_{th}) reduced by 15% in every generation. As we scale down the technology in nanometer scale sever shorter channel effect (SCE) come into existence like DIBL (Drain Induced Barrier Lowering), V_{th} roll off and increase the leakage current[1]. FinNET is the multi gate three dimensional transistors in which gate is wrapped over the thin silicon fin. The two electrically coupled gates and thin silicon fin body suppress the shorted channel effect in sub 22nm and beyond [2-4]. Enhance the control over the to mitigate the shorter channel effect, suppress the leakage current like sub-threshold and gate oxide leakage current will reduces the overall power consumption and improve the performance significantly. The fin body of a double-gate device is typically undoped or lightly doped, therefore enhancement of the carrier mobility and the device variations due to doping fluctuations are reduced in a double-gate FinFET as compared to a single-gate MOSFET. The main difference exists between FinFET and bulk-CMOS appears when larger device are required.

II. FINFET TECHNOLOGY

Many challenges face by FinFET technology as we scale in nanometer regime like random dopant fluctuation (RDF), geometry of the device, capacitance, wrapping of the gate device and many more parameters [5-6]. The main object of the FinFEt technology is to increase the I_{ON} current and mitigate I_{OFF} current for maintain the electrical characteristics in the development of projects and EDA tools for FinFET technology.

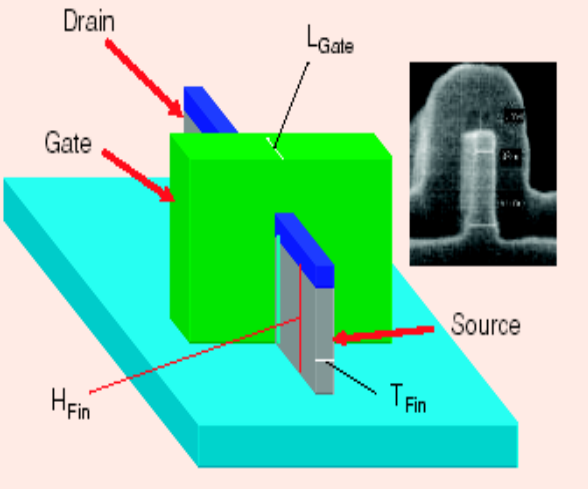

Fig.1. FinFET/Multigate structure

In Fig.1 L represents the length of the FinFET which is similar to the planar FET, the device width W is quite different. W is the width it can be defined as[7]

$$W = 2H_{fin} + T_{fin}$$

where H_{fin} and T_{fin} are the fin height and thickness respectively. Fig.2. represent the top view of the FinFET which shows front gate and back gate of the FinFET. On the surface, this freedom in the vertical direction (of increasing H_{fin}) is a much desired capability since it lets one increase the device width W without increasing the planar layout area! (Increasing W increases the I_{on}, a desirable feature) [8-10].

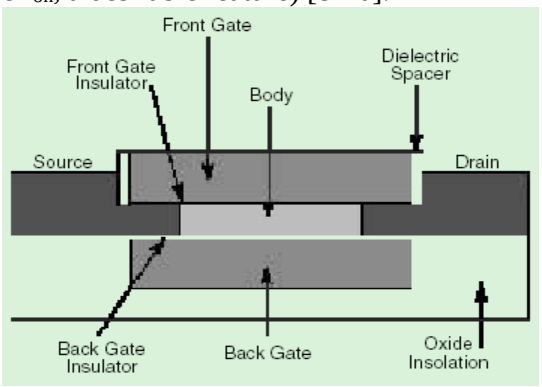

Fig.2. Top View of FinFET

Table .1. Device Technology Parameters [11]

Parameter	Value	
Channel length(L)	32nm	45nm
Effective channel length(L_{eff})	25.6nm	26.4nm
Fin thickness(t_{si})	8nm	8.4nm
Fin height(H_{fin})	32nm	45nm
Oxide thickness(t_{ox})	1.6nm	1.5nm
Source/drain doping (N-type and P-type FinFETs)	$2x10^{-20}$ cm^{-3}	$2x10^{-16}$ cm^{-3}
Supply voltage(V_{DD})	0.8 V	1.0 V

III. Conventional Gates

In this paper we analyze the behavior of different gate in CMOS and FinFET technology we calculate the average power and delay of the gates. Two input NAND gate depend upon the input vector if either input is zero output is one [12]. This logic gate is used to implement other gates in CMOS and FinFET technology. Fig.3, 4, 5, 6, 7 and 8 shows the FinFET based NAND, NOR, AND, XOR and XNOR gate in SP and LP mode of FinFET technology.

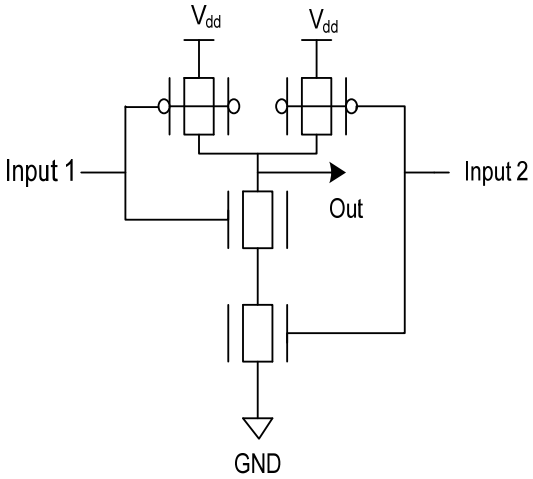

Fig.4. Two input NAND gate

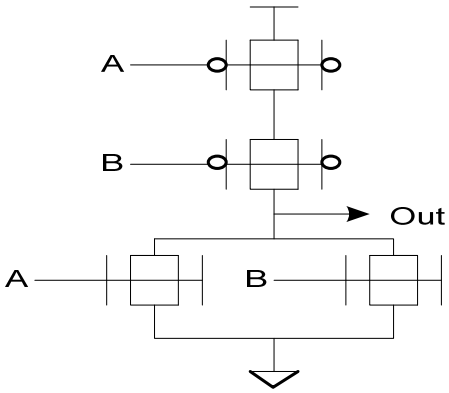

Fig.5. Basic NOR Gate

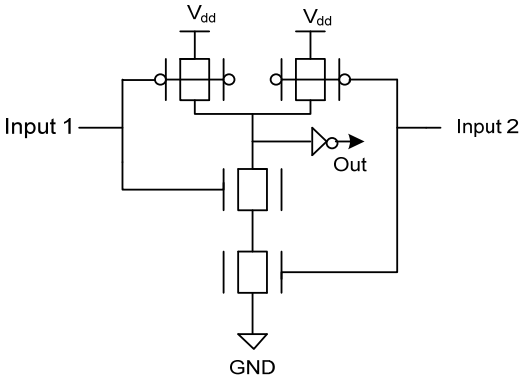

Fig.6. Basic AND Gate

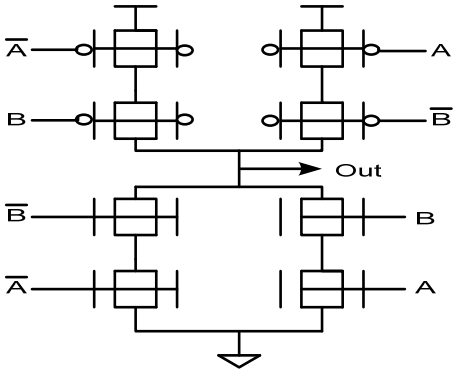

Fig.7. Basic XOR Gate

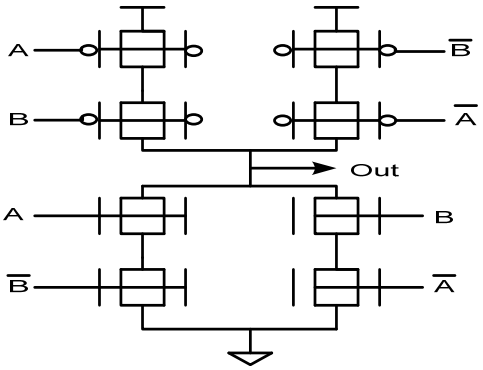

Fig.8. Basic XNOR Gate

IV. Results and discussion

In this section we will discuss the comparison of all the gates in CMOS and FinFET technology and analyse the power and delay calculation. All simulation is performed using HSPICE simulator at 32nm technology with supply voltage of 1V at 25^0C and 110^0C with operating frequency of 10MHZ at C_L= 1pf in SP and LP modes of FinFET technology.

Table II. Comparison of Dynamic Power, Delay and Static Power in SP mode of FinFET

		SP Mode			
		Average Power	Delay	PDP	Static Power
NOT	25^0C	0.226	2.129	0.255	8.968
	110^0C	0.820	1.757	1.435	98.71
NOR	25^0C	0.241	3.586	0.859	16.82
	110^0C	0.734	3.472	2.546	194.6
AND	25^0C	0.454	5.832	2.647	14.80
	110^0C	1.875	9.755	18.29	383.1
NAND	25^0C	0.253	6.516	1.648	0.640
	110^0C	1.134	6.837	7.753	9.966
EXOR	25^0C	0.381	9.414	3.586	16.65
	110^0C	1.489	8.946	13.32	189.6
EXNOR	25^0C	0.372	8.694	3.234	17.67
	110^0C	1.384	8.536	11.81	188.5

Table III. Comparison of Dynamic Power, Delay and Static Power in LP mode of FinFET

		LP Mode			
		Average Power	Delay	PDP	Static Power
NOT	25^0C	0.0391	2.529	0.098	2.741
	110^0C	0.1992	2.432	4.844	38.85
NOR	25^0C	0.1325	11.87	1.572	4.380
	110^0C	0.3426	10.25	3.511	51.46
AND	25^0C	0.3143	15.1	4.774	0.478

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	110^0 C	0.6940	14.83	10.29	20.84
NAND	25^0C	0.2127	12.92	2.748	0.158
	110^0 C	0.4687	12.82	6.008	3.973
EXOR	25^0C	0.2750	19.81	5.274	4.323
	110^0 C	0.5590	18.88	10.55	5.964
EXNOR	25^0C	0.2714	18.34	4.977	4.386
	110^0 C	0.5598	17.49	9.790	49.92

V. Conclusion

In this paper we reviewed the limitation of CMOS circuit; in different basing gates we observe that ultra thin silicon fin of the FinFET drastically suppress the shorter channel effect. FinFET circuits lower optimal energy consumption compared to CMOS circuits and drastic saving of the power consumption and delay. Comparison of CMOS technology FinFET device show drastic improvement in power reduction by 49.38% achieved respectively. From the paper we have concluded that the FinFET-based circuit designs are much lower leakage power consumption and robust than the bulk CMOS counterparts.

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