HIGH FREQUENCY AND AREA EFFICIENT DIGITAL CONTROLLED OSCILLATOR USING NAND GATES

[1]Anju Gupta, [2]Dr.R.S.Pande
Assistant Professor, Shri Ramdeobaba college of Engineering and Management , Nagpur
Professor, Shri Ramdeobaba college of Engineering and Management , Nagpur
[1]guptaam@rknec.edu

Abstract— **This paper reviews on different techniques used to increase the range and frequency of DCO of the all phase locked loop PLL which is the main Requirement of the todays era. The new techniques should be required to reduce the power consumption and for increasing the frequency range .In this paper three transistor based NAND gate is used to design digital controlled oscillator. . Three bit three stage ring DCO with NMOS network gives output frequency [3.39 – 5.35] GHz with power consumption of [0.308 – 0.471] mW. five bit three stage ring DCO with NMOS network gives output frequency [3.65 – 6.11] GHz with power consumption of [0.304 – 0.469] mW. Three bit five stage DCOs with NMOS network shows output frequency of [2.31 – 3.19] GHz with power consumption of [0.534 – 0.672)mw. It is found that increasing the no of bits increases the frequency range as compared to increasing the no of stages.**

Index Terms— DCO,PLL,NMOS

I. INTRODUCTION

The wireless communication industries has grown tremendously in recent years, leading to strong demand for faster ,smaller low consuming circuits. Frequency synthesis is the part of the wireless system. Phase locked loops are widely used in frequency synthesis applications [1], [2].

For many portable applications such as mobile and laptop the acquisition time of PLL is very important so the design of PLLs with minimum acquisition time is the primary goal of this work .A Phase Locked Loop (PLL) is a feedback system that compares the output phase with the input phase to produce an output signal that has the same phase as that of an input signal. PLL's are found in many applications such as reference generation, frequency synthesis, frequency multiplication, FM demodulation etc. As the frequency of operation increases, the need of generating signals that are in phase lock with input (i.e. Fast varying signals) is becoming a problem. There are two types of PLL's 1.Analog PLL 2.Digital PLL. Analog PLL consists of

phase detector, charge pump ,loop filter ,voltage controlled oscillator and frequency divider. But analog PLL has many limitations such as difficult to integrate with design, low speed, occupy large chip area, power consumption, very sensitive to noise, stability . The second type of PLL contains phase frequency detector time to digital converter digital controlled oscillator and frequency counter. Digitally controlled oscillators (DCOs) are the replacement of analog voltage control oscillators (VCOs) in digital PLL systems [6]-[9]. These type of PLL is known as All phase dial phase locked loop DPLL systems which has fast frequency locking, full digital control and good stability [5]. In deep submicron CMOS technology fully digital control oscillators have

become highly attractive circuit components. Different designs for digital controlled oscillators have been reported over varied operating frequency range. In the design delay elements are arranged in ring structure [8], [10], [11]. The Schmitt trigger current driven Digital controlled oscillators [7] , [9], require large number of MOS transistors. Current starved ring oscillators consume large area and with more hardware complexity requires large area [5], [8].

Delay element is important element of the oscillator. The different techniques are used to implement it as reported in literature [12] Two parameters modulate the output frequency of ring oscillator structure. One is propagation delay time of each delay stage and second is total number of delay stages in close ring structure. In DCO structures the oscillating frequency is determined by digital input vector applied to DCDE. Controls switch network of NMOS/PMOS transistors are placed at the sources/drain of NMOS/PMOS transistor of inverter delay cell. Depending upon the condition of input vector, the equivalent resistance of switch network changes and delay of particular stage changes which further modulates the output frequency [5].

In recent years power consumption and output frequency range have become significant performance criteria [12] in DCO system design. Increasing demand of handheld devices like cellular phones, notebooks, personal communication devices have aggressively enhanced the attention for power efficiency. In battery operated communication systems power consumption has also become more significant factor due to exponential increase in data rates. Power consumption in very large scale integration (VLSI) systems includes dynamic, static power and leakage power. Dynamic power consumption results from switching of load capacitance between two different voltages and is dependent on frequency of operation. Static power is contributed by direct short circuits current component between supply (Vdd) & ground (Vss) and it is dependent on leakage currents components. Controlled oscillator is the major components of PLL system and also accountable for most of the power consumption of PLL system. The operating frequency can be increased with more capacitance loading which further adversely affects the total power consumption of oscillator. At circuit level power efficiency can be improved with an optimized design. Optimization are possible in different ways like reduction of switching activity, capacitance and by reducing the short circuit currents etc. This paper proposes novel DCO circuits with NAND gate based inverter delay cell used in ring topology. Here, switch network of transistors are added with inverter based delay cell to control the oscillator frequency. Proposed DCO circuits avoid the analog tuning voltage control and provide the design flexibility with higher power efficiency.

This paper is organized as follows: first section describes delay cell using three transistor NAND gate based three stage DCO .Section II describes 5 stage NAND gate based DCO. Simulation results and discussion have been described in section III. Section IV concludes the work.

II DCO DESCRIPTION

Digitally controlled delay elements (DCDE) are the heart on any DCO structure. The designs of DCO in this paper are based on digitally controlled inverter delay elements connected in ring topology. Three transistor NAND gate working as inverter has been utilized as delay element [3],[4]. One input terminal of NAND gate is connected to Vdd and input signal is applied to second terminal and this circuit works as an inverter. Binary weighted MOS transistors as shown in fig. 1 have been used in switch networks and delay of each stage has been controlled by binary bits applied to these transistors. With changing bit patterns different transistors are selected with unequal width and resistance of transistor network changes accordingly which further modulates the delay of circuit. Changing delay produces different frequency components as controlled by digital input word.

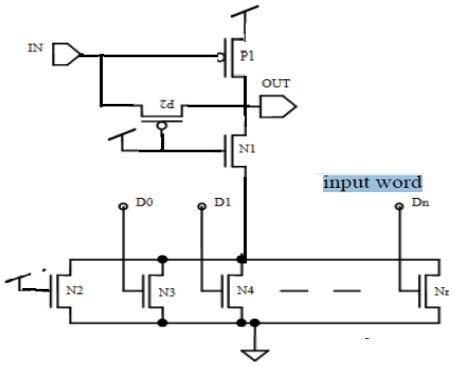

Fig. 1 Delay Cell with NMOS switch network

The delay cell has been proposed using NMOS switching networks as shown in fig. 1. Number of bits can be increased or decreased as per the need of frequency tuning. Gate length of all transistors has been taken as 0.18µm. In NAND based inverter section, width of P1 and P2 has been taken as 1.26µm whereas width of N1 has been taken as 0.24µm. DCO structure with three delay cells having 3-bit control has been shown in figure 2. Switch networks having four NMOS transistors are connected with source terminal of transistor N1 of each delay cell. Four NMOS transistors [N2-N5] are binary weighted with first transistor having Vdd supply at gate terminal to provide path for current conduction. Three control bits [D0-D2] are applied to three binary weighted NMOS transistors [N3-N5].

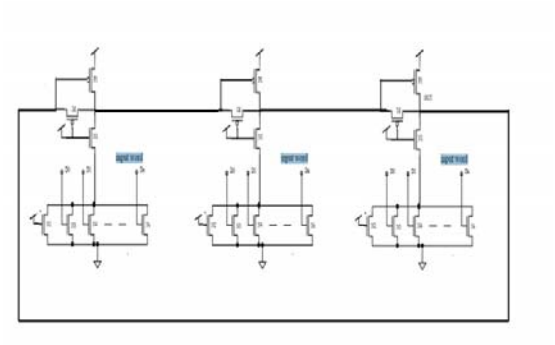

Fig. 2. 3 stage Delay cell with three bit control

III .RESULTS AND DISCUSSIONS

The results have been obtained using Microwind 2.3d software with 180 nm process technology with supply voltage of 1.2V. Power consumption and output frequency has been obtained with different control bits [000 - 111]. In 3-bit NMOS switch network DCO the resistance decreases with varying bit pattern from 000 to 111 and the delay of circuit also reduces. With decrease in delay the output frequency increases with subsequent rise in power consumption. Figure 4 shows the mask layout of 3 bit controlled DCO with NMOS switching network. Tables 1,2,3, show the results of 3-bit controlled DCO,5 bit controlled DCO and 3 bit controlled 5 stage DCO with NMOS switch network. Figures 5,7,9 show the output frequency of 3 bit 3 stage DCO , 5 bit controlled DCO and 3 bit controlled 5 stage DCO.

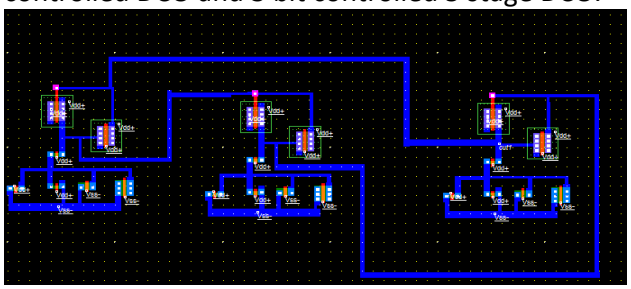

Fig 4 Mask layout of 3 bit controlled 3 stages DCO

Control Word	Frequency(GHz)	Power Consumption
000	3.39	0.308mW
001	4.26	0.379mW
010	4.68	0.415mW
011	4.92	0.438mW
100	5.11	0.454mW
101	5.22	0.460mW
110	5.29	0.466mW
111	5.35	0.471mW

Table 1 3 bit controlled 3 stage DCO

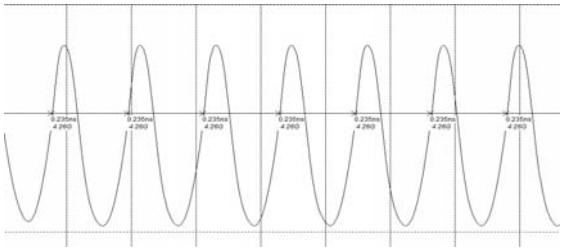

Fig. 5. Output frequency of 3 bit controlled 3 stage DCO

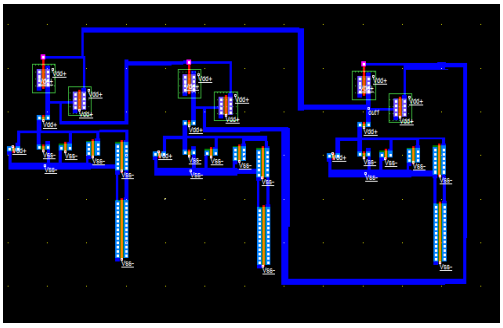

Fig. 6. Mask layout of 5 bit controlled 3 stages DCO

Control Word	Frequency(GHz)	Power Consumption
00000	3.65	0.304mW
00111	5.74	0.469mW
11111	6.11	0.501mW

Table 2. Frequency and power variation with control word for 5 bit controlled 3 stage DCO

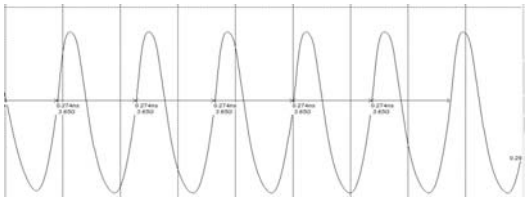

Fig.7. Output frequency of 5 bit controlled 5 stage DCO

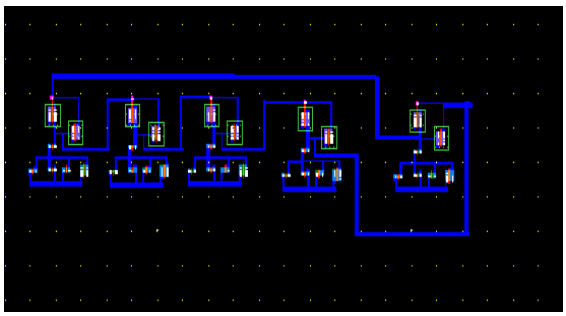

Fig. 8. Mask layout of 3 bit controlled 5 stages DCO

Control Word	Frequency(GHz)	Power Consumption
000	2.31	0.534mW
011	2.99	0.632mW
111	3.19	0.672mW

Table 3. frequency and power variation with control word for 3bit controlled 5 stage DCO

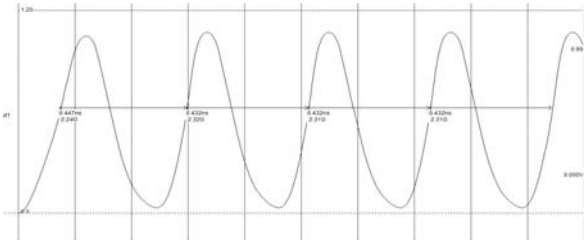

Fig 9. Output frequency of 3 bit controlled 5 stage DCO

IV. CONCLUSION

The new structures for digital controlled oscillators (DCOs) with NAND gates based delay cell having full digital control are reported in this paper. Three, and five bit controlled DCO have been implemented with proposed delay cells. Resistance of switch network has been varied by digital control bits and delay of circuit has been modulated. Three bit three stage ring DCO with NMOS network gives output frequency [3.39 – 5.35] GHz with power consumption of [0.308 – 0.471] mW. five bit three stage ring DCO with NMOS network gives output frequency [3.65 – 6.11] GHz with power consumption of [0.304 – 0.469] mW. Three bit five stage DCOs with NMOS network shows output frequency of [2.31 – 3.19] GHz with power consumption of [0.534 – 0.672] mW. From this it is concluded that dco implementation using NAND based increases the frequency range but at the cost of increase in power consumption.

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