ALGORITHM FOR POWER MINIMIZATION IN SCAN SEQUENTIAL CIRCUITS

[1]Harpreet Singh, [2]Dr. Sukhwinder Singh
[1]M.E. (VLSI DESIGN), PEC University of Technology, Chandigarh.
[2]Professor, PEC University of Technology, Chandigarh
Email: [1]harpreetsingh20789@gmail.com

.

***Abstract*— The paper describes a *An ATPG* technique is proposed that reduces heat dissipation during testing of sequential circuits that have full-scan. The technique increases the correlation between successive states, during shifting in test vectors and shifting out test responses by reducing spurious transitions during test application. The reduction is achieved by freezing the primary input part of the test vector until the smallest transition count is obtained which leads to lower power dissipation. The paper presents a new algorithm which determines the primary input change time, such that maximum saving in transition count is achieved with respect to a given test vector and scan latch order. It is shown how combining the proposed technique with the recently reported scan latch and test vector ordering yields further reductions in power dissipation during test application.**

Keywords*— *Scan ,Scan DFlip-Flop ,DFTAdvisor

I. Introduction

It is important to minimize the power dissipation in VLSI circuits to improve the reliability and reduce packaging costs. There are many techniques to reduce the power dissipation during the normal (functional) mode of operation [2, 4, 8, 12, 13, 17–19], but it is essential to examine and reduce the power dissipation during the test mode of operation due to the following two reasons. Firstly, because the power dissipated during test application is substantially higher than power dissipated during functional operation which can decrease the reliability of the circuit under test due to higher temperature and current density. Secondly, the excessive power/ground noise caused by the high rate of current flowing in power and ground lines can erroneously change the logic state of circuit lines causing some good dies to fall the test [21] leading to yield loss. Depending on level of abstraction and circuit type, high power dissipation during test application is due to the following:

a. The systems which comprise modern memory systems and multichip modules (MCMs) employ power-conscious architectural decisions where blocks are not simultaneously activated under functional operation [7]. Hence, inactive blocks do not contribute to power dissipation during the functional operation. However, when the system is in the test mode of operation, concurrent execution of tests in many blocks will result in substantially higher power dissipation when compared to functional operation.

b. Low power combinational circuits are synthesized by algorithms [2, 12, 17, 18] which seek to optimize the signal or transition probability of circuit nodes using only the spatial dependencies inside the circuit assuming the transition probabilities of primary inputs to be given. However, the complex correlations which occur at the

primary inputs must be considered [16]. The low correlation between consecutive test vectors during test application leads to substantially higher power dissipation when compared to functional operation.

c. Low power sequential circuits are synthesized by state assignment algorithms which use state transition probabilities [4, 8, 17, 19]. The state transition probabilities are computed assuming input probability distribution and state transition graph which is valid during functional operation. These two assumptions are not valid during the test mode of operation when scan design for testability (DFT) technique is employed. Furthermore, in the test mode scan registers are assigned uncorrelated values which are never reached during functional operation leading to substantially higher power dissipation.

To overcome the problem of high power dissipation during test application at the system level, a power-constrained test scheduling algorithm has been proposed for high performance memories and multichip modules [7]. The algorithm is based on a resource graph formulation for the test problem and tests are scheduled concurrently without exceeding their power ratings during test application. A new ATPG tool [21] was proposed to overcome the low correlation between consecutive test vectors during test application in combinational circuits. A different approach for minimizing power dissipation during test application in combinational circuits is based on test vector ordering [9]. To minimize power dissipation in scan sequential circuits during test application two techniques have been proposed [9, 10]. In [10], the modules and modes with the highest power dissipation are identified, and gating logic to reduce power dissipation has been proposed. Despite substantial savings in power dissipation gating logic introduces not only supplementary area overhead but also performance degradation. The technique in [9] is based on test vector and scan latch ordering increases the correlation between consecutive states during shifting in present state part of the test vector and shifting out test responses. However, the technique proposed in [9] is test vector and scan latch order dependent and cannot significantly reduce power dissipation despite a large computational time required to explore the large design space. Furthermore, for circuits with large number of scan latches the technique pro-posed in [9] is infeasible since computational time required to compute the cost function of each solution in the large design space, is unacceptably large.

The aim of this paper is to introduce a new technique for power minimization during test application in full scan sequential circuits which eliminates the computational overhead associated with test vector and scan latch ordering [9]. The technique is based on partitioning scan latches into multiple scan chains and applying an extra test vector to primary inputs while shifting out test responses for each scan chain. This paper shows that with low test area and test data overhead high savings in power dissipation during test application in large full scan sequential circuits are achieved in low computational time.

I. The Previous work

To reduce the switching activity during scan shift, automatic test pattern generation (ATPG)-based approach and DFT-based approach were used. The advantage of the ATPG based solutions is that they do not modify the original design and the scan architecture, but modification is done on test vectors and there by power reduction can be obtained. DFT-based solutions require one to either partition the conventional scan chain architecture or insert additional hardware into the design. In Minimized power consumption for scan based Bist, extra logics are inserted to hold the outputs of all the scan cells at constant values during scan shifting. This method not only minimizes the average scan shift power, but also avoids peak power hazards during scan shifting. The main disadvantage of these approaches is the large area overhead, since additional logics are added to all the scan cells. Moreover, it may degrade circuit performance due to extra logics added between scan cell outputs and functional logics. To reduce the area overhead due to additional gates, supply gating transistors for the first-level gates at the outputs of scan cells are proposed in Low power scan design using first level supply gating. An alternative implementation

to hold the scan cell outputs by using dynamic logic was proposed in Techniques for minimizing power dissipation in scan and combinational circuit during test application. The method proposed in Inserting test points to control peak power during scan testing, inserts test points at selected scan cell outputs to keep the peak shift power at every shift cycle below a specified limit. Given a set of test patterns, logic simulation is carried out to identify the shift cycles in which peak power violations occur. Those cycles are called violating cycles. By using integer linear programming (ILP) techniques, the optimization problem is solved to select as few test points as possible such that all violating cycles can be eliminated. In Partial gating optimization for power reduction during test application, random vector simulation was used to guide partial test point selection. When simulating a random vector, the primary inputs and the pseudo primary inputs are changed to value X with pre-specified probabilities, and the number of gates becoming X after the change is used as a cost function to identify the logic value assigned at the primary inputs and the pseudo primary inputs, as well as to select scan cells to be held during scan shifting. To explore several hundred thousands of scan cells in an industrial circuit, a significant number of random vectors need to be simulated in order to choose good test points. Motivated by the test point insertion approach along with multiple scan chain, scan shift power can be reduced to a larger extend. Some scan cells have a much larger impact on toggle rates at the internal signal lines than other scan cells. These scan cells are called power sensitive scan cells. Objective is to quickly identify power sensitive scan cells and their preferred frozen values during scan shifting. By freezing a small percentage of scan cells that are the most power sensitive, reduction in scan shift power can be achieved, while minimizing the additional area overhead. Compared with the previous approaches, this approach has less area overhead and can avoid modifying scan cells at critical paths by not selecting them to freeze. This approach also provides a practical way to handle large industrial designs and since both freezing power sensitive scan cells and multiple scan chain approach is used, power can be reduced to a larger extend.

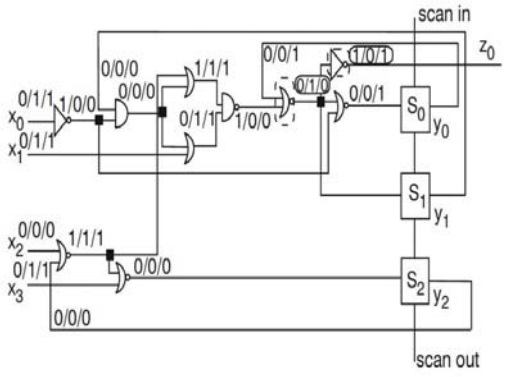
II. Power Dissipation Model

Power dissipation in CMOS circuits can be divided into static, short-circuit, leakage and dynamic power dissipation. The static power dissipation is negligible for correctly designed circuit, short-circuit power dissipation caused by short-circuit current during switching and power dissipated by leakage currents, contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs [12]. If the gate is part of a synchronous digital circuit controlled by a global clock, it follows that the dynamic power P_d required to charge and discharge the output capacitance load of every gate is given by

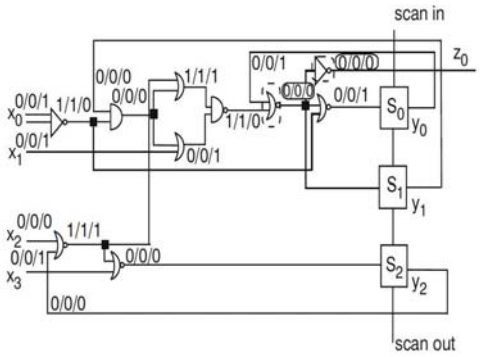
$$P_d = 0.5 \times C_{load} \times (V_{DD}^2 / T_{cyc}) \quad \ldots(1)$$

where C_{load} is the load capacitance, V_{DD} is the supply voltage, T_{cyc} is the global clock period and N_G is the total number of gate output transitions (0 → 1 or 1 → 0). The vast majority of power reduction techniques concentrate on minimizing the dynamic power dissipation by reducing one or more variables of P_d. The supply voltage V_{DD} is usually not under designer control and global clock period T_{cyc} or more generally, the system throughput is a constraint rather than a design variable. Thus, node transition count (NTC)

$$NTC = \sum_{\text{for all gates } G} N_G \times C_{load} \quad \ldots(2)$$

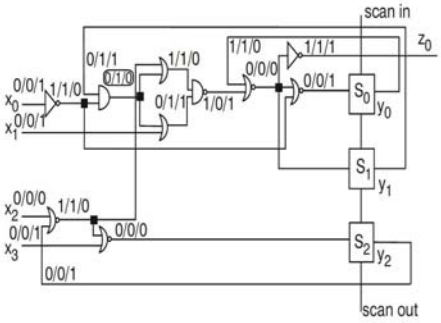


a

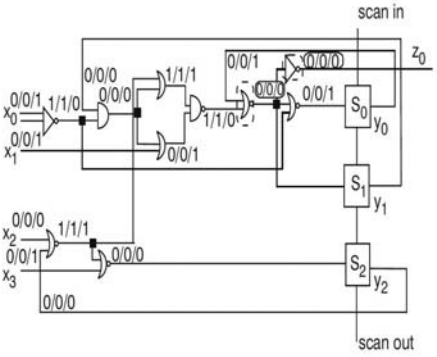


b

Fig.1Example circuit (s27 from [13]) illustrating factors which lead to spurious transitions during test application a Primary inputs change as soon as possible(ASAP) at t_0 b Primary inputs change at t_1



a



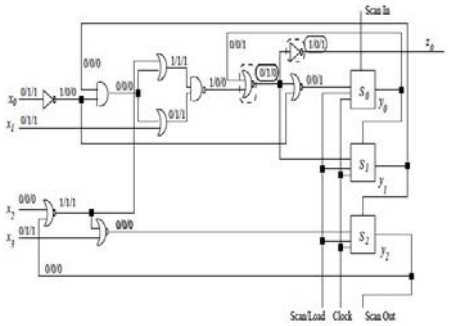
b

Fig. 2 Example circuit (s27 from [13]) illustrating factors which lead to spurious transitions during test application a Primary inputs change as late as possible (ALAP) at t_3 b Primary inputs change at t_2

is used as a quantitative measure for power dissipation throughout the paper. It has been assumed that load capacitance for each gate is equal to the number of fan-outs. The node transition count in scan latches N_{SL} is considered as in [11], where it was shown that, for input changes 0→0 and 1→1, N_{SLmin} =2, while, for input changes 0→1 and 1→0, N_{SLmax} =6

III. Minimization of Power Dissipation During Test Application By Controlling Primary Input Change Time

To motivate the need for a new test application strategy for power minimization, an overview of testing scan sequential circuits is provided. For a scan sequential circuit, each test vector $V_i = x_i@y_i$ applied to the circuit under test is composed of primary input part *xi* and pseudo input y_i, where @ denotes concatenation. Given *m* scan cells, for each test vector $V_i = x_i@y_i$ the present state part y_i is shifted in *m* clock cycles t_0 to t_{m-1}. In the case of partial scan sequential circuits, the non-scan cells preserve their value during clock cycles t_0 to t_{m-1}. In the next clock cycle *tm* the entire test vector $Vi = x_i@y_i$ is applied to the circuit under test. A scan cycle represents the *m*+1 clock cycles t_0 to t_m required to shift in the present state part of the test vector and apply the entire test vector to the circuit under test. In the following *m* clock cycles of the next scan cycle the test response y_0 *i* is shifted out simultaneously with shifting in the present state part of the next test vector $V_j = x_j@y_j$. The values of the primary inputs are important only at *tm* when the entire test vector is applied. Therefore the primary inputs can be changed at clock cycles t_0 to t_{m-1} without affecting test efficiency. The transitions which occur in the circuit combinational part, without any influence on test efficiency or test data, are defined as follows.



(a) Primary inputs change as soon as possible (ASAP) at *t*0

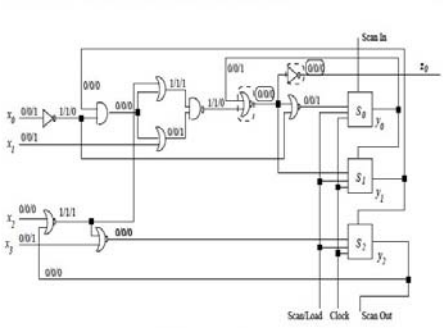
Figure 3.6: Example circuit (*s27* from [23]) illustrating factors which lead to spurious transitions during test application

Definition 3.1 A spurious transition during test application in scan sequential circuits is a transition which occurs in the combinational part

of the circuit under test while shifting out the test response and shifting in the present state part of the next test vector. These transitions do not have any influence on test efficiency since the values at the input and output of the combinational part are not useful test data.

Definition 3.2 The test application strategy where primary inputs change at $t0$ is called *as soon as possible* (ASAP).

Definition 3.3 The test application strategy where primary inputs change at tm is called *as late as possible* (ALAP), where m is the number of sequential elements converted to
scan cells.

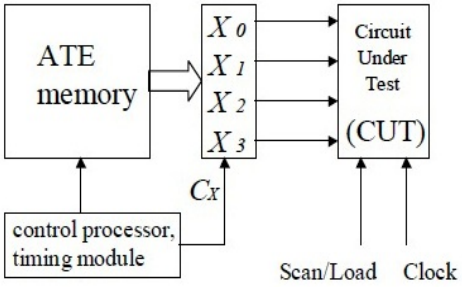


(b)

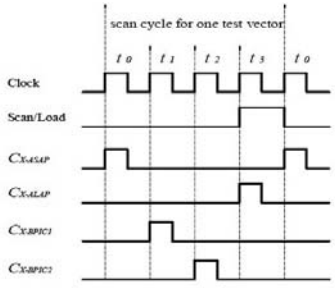
Primary inputs change at $t1$

Figure 3.6: Example circuit (*s27* from [23]) illustrating factors which lead to spurious transitions during test application

Definition 3.4 The best primary input change time of test vector V_j is the time when the primary input part x_i of the previous test vector V_i changes to the primary input part x_j of
the actual test vector V_j, leading to the smallest value of node transition count during the scan cycle when test vector V_j is applied after test vector V_i. Finding the best primary input change time will lead to higher correlation between consecutive values on the input lines of the combinational part of the circuit. This leads to minimum value of *NTC* during the scan cycle, and yields savings in power dissipation.



(a) Interface to ATE



(b)

Different primary input change times

Figure 3.7: Interface to ATE for different test application strategies.

Definition 3.5 The test application strategy where best primary input change time for each test vector V_i, with $i = 0,\ldots,n\text{-}1$, is determined such that the minimum value of node
transition count over the entire test application period is achieved, is referred to as *best primary input change* (BPIC) test application strategy.

II. Algorithm for Minimizing Power Dissipation During Test Application

This section introduces a new and exact algorithm which computes best primary input change time for each test vector with respect to a given test vector and scan cell order. We will also discuss the proposed test application strategy with the recently introduced scan cell and test vector ordering using a simulated annealing-based design space exploration leads to further reductions in power dissipation during test application.

A. *Best Primary Input Change (BPIC) Algorithm*

Spurious transitions induced by fixed primary input changes are solved by changing the primary inputs of each test vector such that the minimum number of transitions is achieved. For a given scan cell order with m scan cells, the total number of primary input change times is $(m+1)$. Considering n test vectors, in a given test vector order, the total number of configurations of primary input changing for all the test vectors is $(m+1)n$. Best Primary Input Change Algorithm (*BPIC-ALG*) computes the best primary input change time for each test vector for a given scan cell order and test vector order. The pseudocode of the proposed *BPICALG* algorithm is given below. The function accepts as input, a test set **S** and a circuit **C**. The outer loop represents the traversal of all the test vectors from test set **S**. All

the m+1 primary input change times for test vector V_i are then considered in the inner loop. For each primary input change time t_j, circuit **C** is simulated and the node transition count $NTC_{i,j}$ is registered. After the completion of the inner loop the best primary input change time t_{Bi}, for which $NTC_{i,Bi}$ is minimum, is retained and the outer loop continues until the entire test set is examined. The algorithm computes the best solution in a computational time which is polynomial in the number of test vectors n, the number of scan cells m, and the circuit size |**C**|. It should be noted that *BPIC-ALG* is *test set dependent* and hence it is applicable only to *to small to medium sized* sequential circuits.

ALGORITHM: **BPIC-ALG**
INPUT: Test Set **S**, Circuit **C**
OUTPUT: Best primary input change times {$\mathbf{t_{B0}, t_{B1},}$……., $\mathbf{t_{Bn-1}}$}
Node transition count over the entire test application period **NTC**

1. **NTC** ← 0
2. **for** every test vector *Vi* from **S** with i = 0 **,**……, n-1 {
3. **for** every primary change time $t_{Vi} = t_j$ with j = 0**,**……,m
4. compute $NTC_{i,j}$ by simulating **C** during the scan cycle when applying *Vi* using the scan cell order {$\mathbf{S_0}$**,**……,$\mathbf{S_{m-1}}$}
5. get best primary input change time $\mathbf{t_{Bi}}$ for test vector V_i such that $NTC_{i,Bi}$ is minimum
6. **NTC** ← **NTC**+$NTC_{i,Bi}$
7. }
8. **return** {$\mathbf{t_{B0}, t_{B1},}$……., $\mathbf{t_{Bn-1}}$}, **NTC**

III. Conclusion

This paper has proposed a new technique for minimizing power dissipation in full-scan sequential circuits during test application. The technique is based on increasing the correlation between successive states, during shifting in test vectors and shifting out test responses, by freezing the primary inputs until the smallest number of transitions is achieved. A new algorithm which computes best primary input change time for each test vector has been presented. It has been shown that combining the described technique with the recently reported scan latch and test vector ordering, using a simulated annealing-based design space exploration, yields substantial reductions in power dissipation during test application. Exhaustive experimental results using both compact and noncompact test sets have shown that compact test sets have similar power dissipation during test application, with substantial reduction in test application and computational time when compared to noncompact test sets.

While this paper has shown how BPIC minimizes power dissipation in full scan sequential circuits, current research underway by the authors investigates the applicability of BPIC to partial scan and the identication of the best design for test method in terms of power dissipation during test application.

References

[1] M. Abramovici, M. Breuer, and A. Friedman. *Digital Systems Testing and Testable Design*. IEEE Press, 1990.

[2] R. Bahar, H. Cho, G. Hachtel, E. Macii, and F. Somenzi. Symbolic timing analysis and resynthesis for low power of combinational circuits containing false paths. *IEEE Trans-actions on CAD*, 16(10):1101–1115, Oct 1997.

[3] P. Bardell, W. McAnney, and J. Savir. *Built-In Self Test - Pseudorandom Techniques*. John Wiley & Sons, 1986.

[4] L. Benini and G. D. Micheli. State assignment for low power dissipation. *IEEE Journal of Solid-State Circuits*, 30(3):258–268, Mar 1995.

[5] F. Brglez, D. Bryan, and K. Kozminski. Combinational profiles of sequential benchmark circuits. In *Proc. Inter-national Symposium on Circuits and Systems*, pages 1929– 1934, 1989.

[6] A. Chandrakasan and R. Brodersen. *Low Power Digital CMOS Design*. Kluwer Academic Publishers, 1995.

[7] R. Chou, K. Saluja, and V. Agrawal. Scheduling tests for VLSI systems under power constraints. *IEEE Transactions on VLSI*, 5(2):175–184, Jun 1997.

[8] S.-H. Chow, Y.-C. Ho, T. Hwang, and C. Liu. Low power realization of finite state machines - a decomposition approach. *ACM Transactions on Design Automation of Electronic Systems*, 1(3):313–340, Jul 1996.

[9] V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy. Techniques for minimizing power dissipation in scan and combinational circuits during test application. *IEEE Transactions on CAD*, 17(12):1325–1333, Dec 1998.

[10] S. Gerstendorfer and H. Wunderlich. Minimized power consumption for scan-based BIST. In *Proc. IEEE International Test Conference*, pages 77–84, 1999.

[11] M. Hsiao, E. Rudnick, and J. Patel. Effects of delay models on peak power estimation of VLSI sequential circuits. In *Proc. International Conference on Computer Aided Design*, pages 45–51, 1997.

[12] S. Iman and M. Pedram. An approach for multi-level logic optimization targeting low power. *IEEE Transactions on CAD*, 15(8):889–901, Aug 1996.

[13] G. Lakshminarayana, A. Raghunathan, N. Jha, and S. Dey. Power management in high level synthesis. *IEEE Transactions on VLSI*, 7(1):7–15, Mar 1999.

[14] H. K. Lee and D. S. Ha. On the generation of test patterns for combinational circuits. Technical Report No. 12-93, Department of Electrical Engineering, Virginia Polytechnic Institute and State University, 1991.

[15] S. Manich and J. Figueras. Maximizing the weighted switching activity in CMOS combinational circuits under the variable delay model. In *Proc. European Design and Test Conference*, pages 597–602, 1997.

[16] R. Marculescu, D. Marculescu, and M. Pedram. Probabilistic modelling of dependecies during switching activity analysis. *IEEE Transactions on CAD*, 17(2):73–83, Feb 1998.

[17] K. Roy and S. Prasad. Circuit activity based CMOS logic synthesis for low power reliable operations. *IEEE Transactions on VLSI*, 1(4):503–513, Dec 1993.

[18] J.-M. Tseng and J.-Y. Jon. Two-level logic minimization for low power. *ACM Transactions on Design Automation of Electronic Systems*, 4(1):52–69, Jan 1999.

[19] C.-Y. Tsui, M. Pedram, and A. Despain. Low-power state assignment targeting two- and multilevel logic implementations. *IEEE Transactions on CAD*, 17(2):1281–1291, Dec 1998.

[20] A. Vital and M. Marek-Sadowska. Low-power buffered clock tree design. *IEEE Transactions on CAD*, 16(9):965– 975, Sep 1997.

[21] S. Wang and S. Gupta. ATPG for heat dissipation minimization during test application. *IEEE Transactions on Computers*, 47(2):256–262, Feb 1998.

[22] Y. Zorian. A distributed BIST control scheme for complex VLSI devices. In *Proc. 11th IEEE VLSI Test Symposium*, pages 4–9, 1993.

[23] "Power Constrained Testing of VLSI circuits" by Nicola Nicolici and Bashir M. Al-Hashimi .