DESIGN AND ANALYSIS OF LOW POWER ADDERS USING SUBTHRESHOLD ADIABATIC LOGIC

S.Soundarya[1], MS.S.Anusooya[2], V.Jean Shilpa[3]
[1]PG student, VLSI and Embedded systems, [2,3]Assistant professor of ECE Dept.
B.S. Abdur rahman university, Chennai,

Abstract

In this works achieves the adders operates in ultra low power. We achieve this ultra low power by using adiabatic logic. Adiabatic logic style is a hopeful method to attain ultra low power. This adiabatic logic of gates having capacitors here the energies stored and recycled. The recycling is done by using reversing the direction of power supply. So that we can reduces the dissipated heat. But in conventional CMOS logic the energies are wasted by connected to the ground. This work shows that SAL- Subthreshold Adiabatic Logic to design the carry skip adder and carry save adder. These two adders are 8-bit adders. Simulation results express that subthreshold adiabatic logic can save large amount of energy compared with a conventional CMOS technology. Results are verified by simulations in 180-nm CMOS technology using CADENCE.

Index Terms: Adiabatic logic, Subthreshold logic, Adders, Ultra low power, Carry skip adder, Carry save adder.

I. INTRODUCTION

A low power VLSI chips become need from such development forces of IC's. In adiabatic logic we used pulsed power supply. In Practically resonant inductor circuits used as power supply. In traditional method Conventional CMOS logic gates used to implement the adders. In charging and discharging produce Dynamic power dissipation (switching0→1,1→0).When switching occurs in the transistors (NMOS and PMOS) are conduct current from supply to ground. It causes heat dissipation. In adiabatic logic gates are designed by less no of transistors and each gate having one load capacitors. While switching process occurs in the adiabatic logic circuits it reduces the energy dissipation by storing the energy into the capacitors and that energy is reclaimed by reversing the power supply phase shown in FIG 1.2. So that the adiabatic logic circuits have pulsed power supply. Here we are using ramp type power supply.

II.SUBTHRESHOLD LOGIC

Given power supply vdd is lesser then the transistors threshold voltage vt is called as subthreshold logic. Using cadence make sure that all the transistors are definitely working in the subthreshold region.

III. PRINCIPLE OF ADIABATIC LOGIC

Thermodynamic process is expressed as adiabatic in greek language. It produces no heat loss and no energy in the environment. Circuits having some dissipative elements like resistance, so that we cannot achieve ideal process in real life. If we reduces the speed of operation we can get very low power dissipation. In adiabatic logic, switching transistors are made of under assured conditions. . This adiabatic logic of gates having capacitors here the energies stored and recycled. The recycling is done by using reversing the direction of power supply. So that we can reduces the dissipated heat. . So that we can reduces the dissipated heat. so that it is called as energy recovery CMOS. Zero energy loss is impossible, but in adiabatic technique,

the circuit energy is conserved, as an alternative of dissipated as heat. This adiabatic technique reduces the power dissipation in digital systems depends on purpose and system needs.

IV. ADIABATIC GATES

In adiabatic technique first we have to implement standard cell library for SAL logic. Library contains common gates, complex gates, special gates are compulsorily implemented for design basic structure of 8 bit carry skip adder and carry save adder. In adiabatic logic restructure the conventional gates that is, in convention method NAND gate is implemented by 4 gates in adiabatic logic NAND gate is designed b y 2 gates. These gates are designed between supply clock and output capacitor.

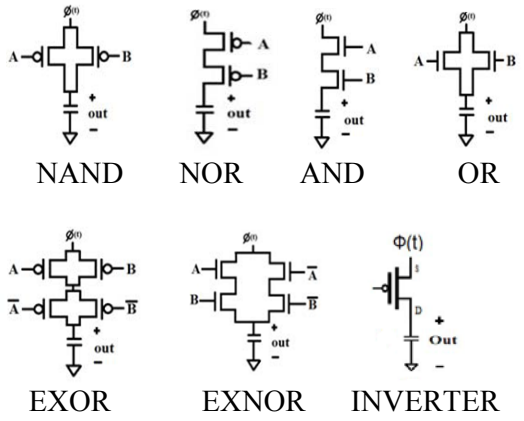


Figure 1: Adiabatic logic based basic gates

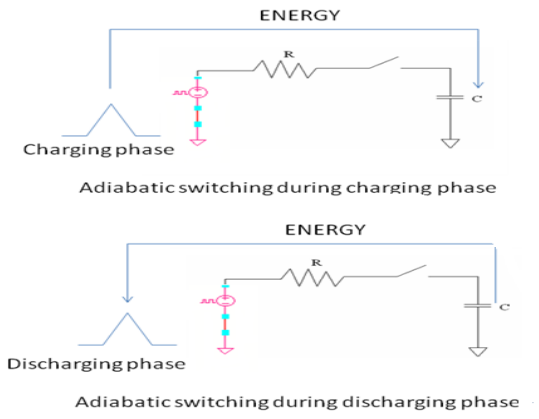


Figure 2: Adiabatic switching

V. BASIC STRUCTURE OF CSkA

This is 8 bit carry skip adder. This adder consists of two blocks one is ripple carry adder block other one is skip chain block. This adder is speeder. In ripple carry adder one full adder input is waiting for another full adder output. So time delay is increased. But in this carry skip chain if the skip chain is detected the 1 means it will automatically skip the operation and it gives the 1 to the next block so it is faster. If no of bits increased this skip adder is most significant.

Each exor gate output is denoted as Pi, Pi+1, Pi+2,Pi+3. Cout is expressed as (Ci+4) + P[i , i+3]. Cin

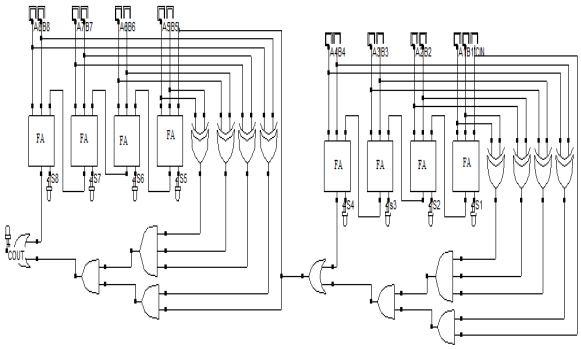


Figure 3: Basic structure of CSkA

VI. BASIC STRUCTURE OF CSaA

This adder is mainly used for reduces the addition of three numbers to addition of two numbers. So the propagation delay is reduced. This adder contains two blocks one is ripple carry adder block and another one is carry save adder block. This ripple carry adder block consists of 8 full adder because this is 8 bit carry save adder. In carry save chain all cin is connected to ground. So it will add partial addition and that partial addition is given into ripple carry adder block that will gives actual sum and carry.

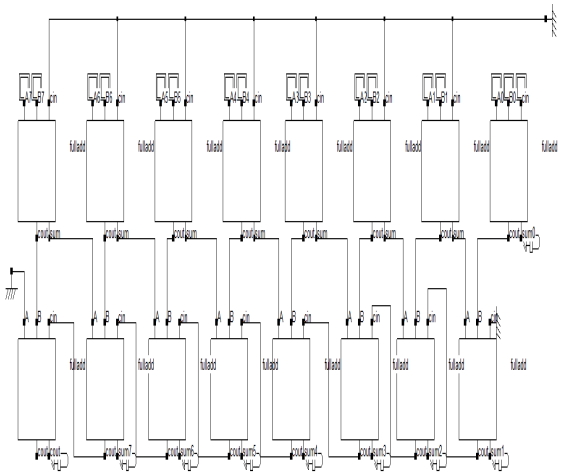


Figure 4: Basic structure of CSaA

VII. EXISTING METHOD
CONVENTIONAL CMOS LOGIC

In conventional CMOS based basic structure of carry skip adder (CSkA) and carry save adder (CSaA) implemented by using conventional CMOS and this method uses constant power supply (VDD). Conventional CMOS logic gate used to implement the CSkA and CSaA.

- More no of the transistors so area increased.
- Temperature leakage is high.(i.e) Heat dissipation is increased.
- Power waste is increased.
- The overall performance of the circuit is very low. so weak operation will occur.
- Delay is more.

CONVENTIONAL CMOS BASED CARRY SKIP ADDER

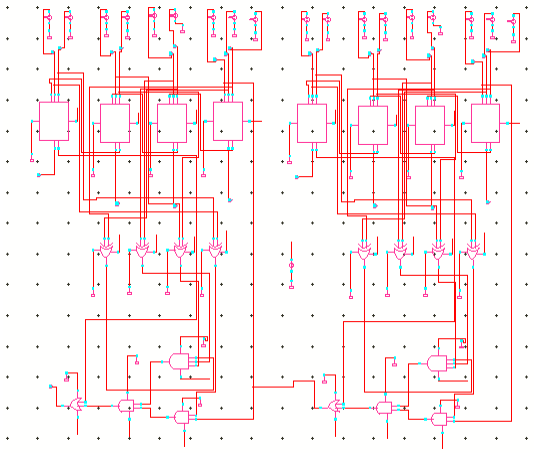
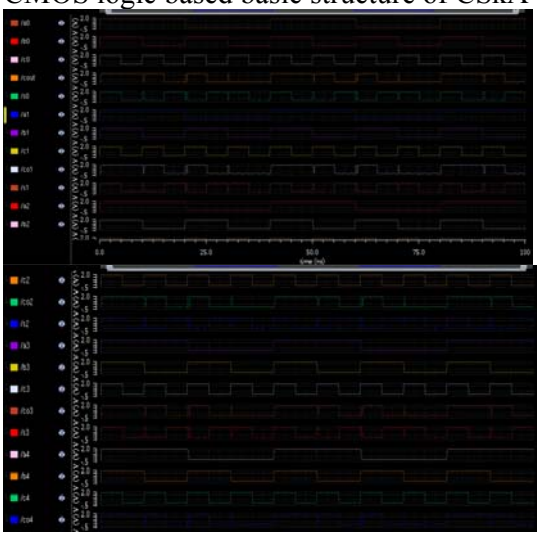


Figure 5: Schematic diagram of conventional CMOS logic based basic structure of CSkA



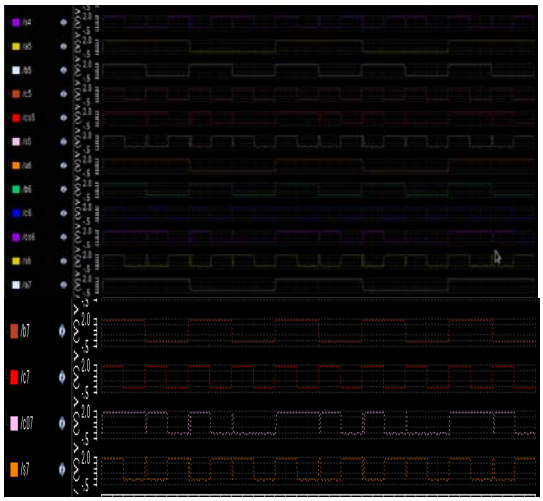


Figure 6: Output waveform of conventional CMOS logic based basic stucture of CSkA

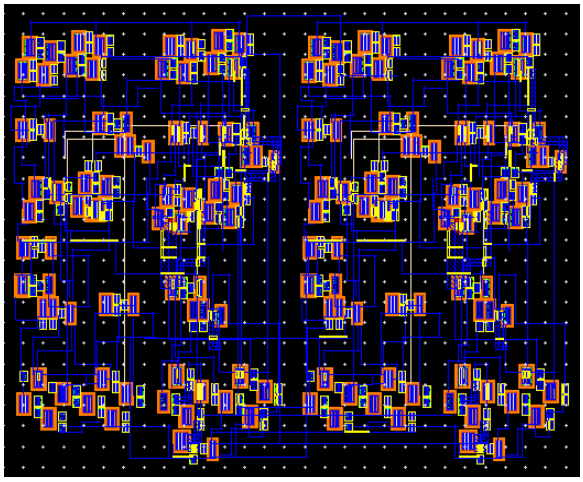


Figure 7: Layout design of conventional CMOS logic based basic structure of CSkA

CONVENTIONAL CMOS BASED CARRY ADDER

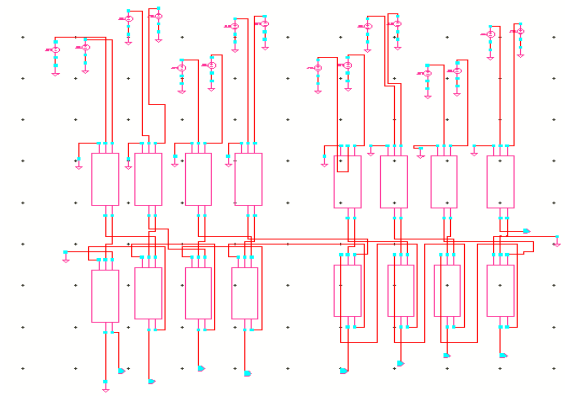


Figure 8: Schematic diagram of conventional CMOS logic based basic structure of CSaA

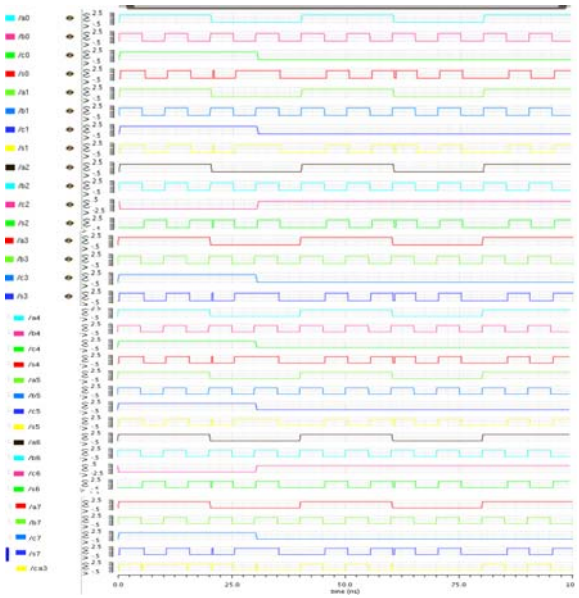


Figure 9: Output waveform of conventional CMOS logic based basic stucture of CSaA

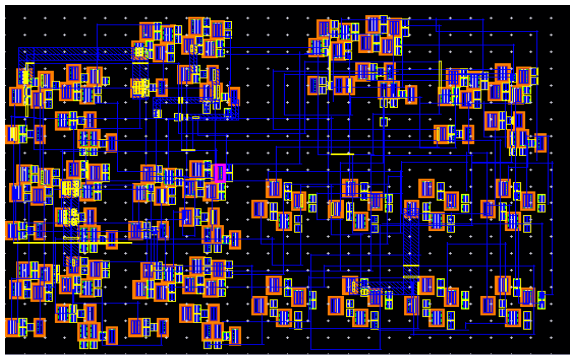


Figure 10: Layout design of conventional CMOS logic based basic structure of CSaA

VIII. PROPOSED METHOD ADIABATIC LOGIC

For adiabatic logic first we have to implement SAL based library. This library consist of logic gates, complex gates, etc. Then using this gates we have to implement digital circuits. In adiabatic logic transistors count approximately half compared to Conventional CMOS logic.

- Comparing to the conventional CMOS logic design method this adiabatic logic transistor count only half.
- The SAL technique can be used to make the circuit have to save energy compared to another method.
- Area is reduced.
- Delay is reduced.
- Reduced heat dissipation.
- Achieved low power so power waste is reduced.

ADIABATIC LOGIC BASED CARRY SKIP ADDER

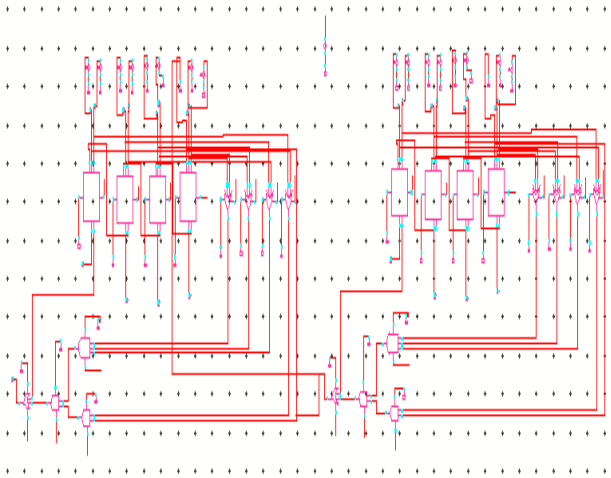


Figure 11: Schematic diagram of SALlogic based basic structure of CSkA

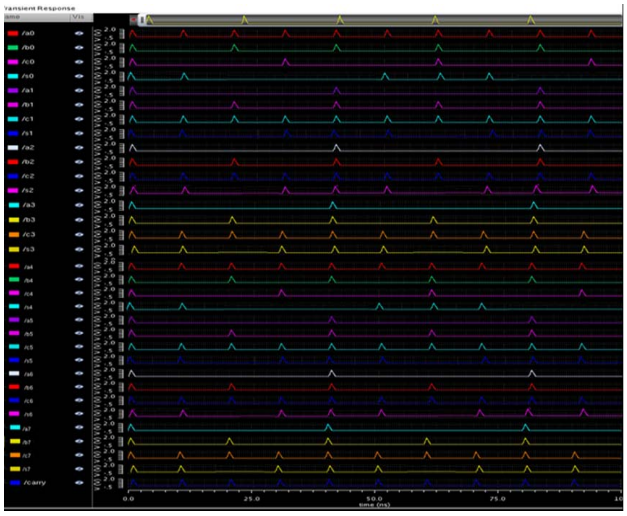


Figure 12: Output waveform of SAL based basic stucture of CSkA

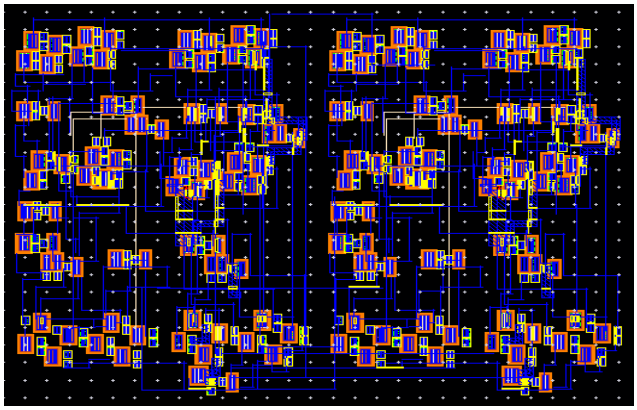


Figure 13: layout of SAL based basic stucture of CSkA

ADIABATIC LOGIC BASED CARRY SAVE ADDER

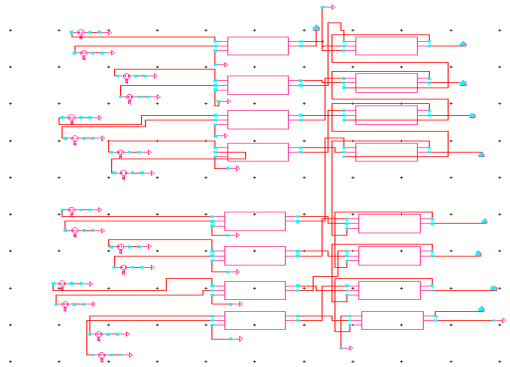


Figure 13: Schematic diagram of SAL logic based basic structure of CSaA

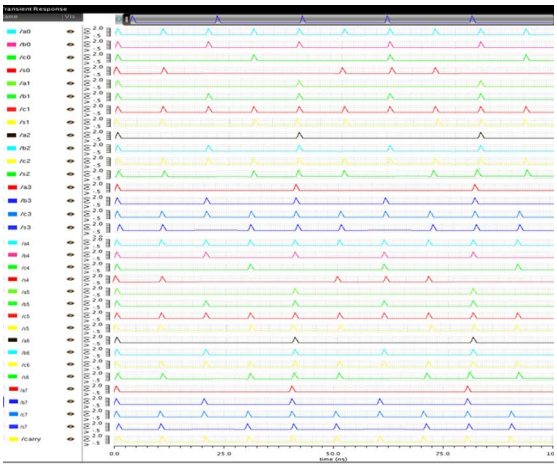


Figure 14: Output waveform of SAL based basic stucture of CSaA

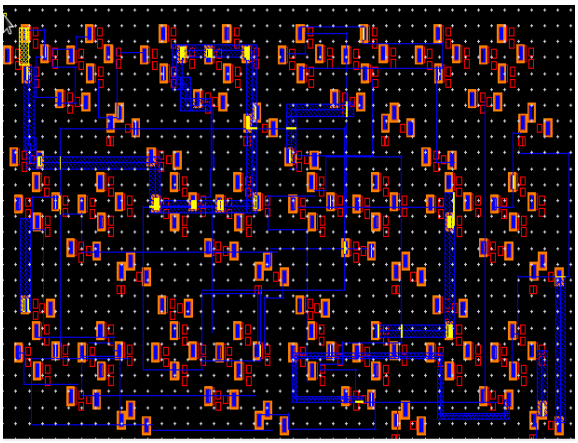


Figure 14: layout of SAL based basic stucture of CSaA

TYPES OF ADERS	POWER CONSUMPTION	DELAY CALCULATION	AREACALCULATION
Conventional CMOS	3.339 µW	0.7603 ns	5912.68 µ m^2
Logic based carry look ahead adder			
Adiabatic logic based carry look ahead adder	1.223 µW	0.42ns	4083.25 µ m^2
Conventional CMOS logic based carry skip adder	4.2 µW	0.495 ns	16282.61 µ m^2
Adiabatic logic based carry skip adder	2.24 µW	0.14 ns	13818.52 µ m^2
Conventional CMOS logic based carry skip adder	5.07 µW	0.495 ns	32040.34 µ m^2
Adiabatic logic based carry skip adder	3.56 µW	0.137 ns	22953. 536 µ m^2

Table 1: Performance Comparison

IX. APPLICATIONS

- Adiabatic logic is used in low power CMOS circuits. Adiabatic logic has been useful to power minimization VLSI systems.
- This adiabatic logic can be used in future energy-saving devices.

- Subthreshold circuits will suitable for which necessarily needs very low power utilization (e.g portable electronic devices).

REFERENCES

[1] Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application, Manash Chanda, Sankalp Jain, Swapnadip De, Chandan Kumar Sarkar, "IEEE transactions on very large scale integration (vlsi) systems", 2015.

[2] A 0.25 V 460 nW asynchronous neural signal processor with inherent leakage suppression, T.-T. Liu and J. M. Rabaey, "IEEE J. Solid-State Circuits", vol. 48, no. 4, pp. 897–906, Apr. 2013.

[3] Design techniques and architectures for low-leakage SRAMs, A. Calimera, A. Macii, E. Macii, and M.Poncino, "IEEE Trans. Circuits Syst. I", Reg. Papers, vol. 59, no.9, pp. 1992–2007, Sep. 2012.

[4] Analysis and design of an efficient irreversible energy recovery logic in 0.18-µm CMOS, C.-S. A. Gong, M.-T. Shiue, C.-T. Hong, and K.-W. Yao, "IEEE Trans. Circuits Syst. I, Reg. Papers", vol. 55, no. 9, pp. 2595–2607, Oct. 2008.

[5] Robust subthreshold logic for ultra-low power operation, H. Soeleman, K. Roy, and B. C. Paul, "IEEE Trans. Very Large Scale Integr. (VLSI) Syst", vol. 9, no. 1, pp. 90– 99, Feb. 2001.